Octopus™ 8-Port DRAM for Die-Stack Applications — High-Speed L3 with ECC

Features

- Capacity: 1Gb to 4Gb
- Latency: as little as 7ns
- Maximum clock rate: 800MHz
- Minimum Timing: tRCD=2, tCYC=6, tPCR=4, tCL=2
- 8 ports x 128 bits each direction
- Programmable burst length: 4 or 8
- DDR 1600MT Max
- Sustainable 50 GB/sec in closed page mode with BL=4
- 200GB/s peak bandwidth
- Multiplexed address
- Max Cio 0.25pf
- Max Cclk 0.8pf
- Unidirectional data flow between memory and host
- 1.4V to 1.7V I/O, 1.4V to 1.7V Core
- Max core current 1.3A, Nom 800mA
- Internally ECC protected by Bit Armor™
- JTAG configuration/test/status port
- "Mailbox" interface for configuration & testing
- 115ºC full function operating temperature
- Memory to Host I/O, Vdd, Vss interconnect organized in 64 x 10 contact block per port (8 contact blocks per part)
- Inter-die contacts: 10um pads on 25um center
- 21.8 x 12.3 mm die footprint

Options

Options		Marking
Configurations:	1 Gbit	TSC100801
	2 Gbit	TSC100802
	4 Gbit	TSC100804

Functional Description

The Tezzaron Octopus™ is designed to bring an entirely new level of performance to next generation processing devices. Designed for intimate integration using die-to-die or die-to-wafer bonding technologies, the Octopus can significantly boost overall system throughput.

The Octopus provides superior L3 caching with unprecedented density and reliability; it can deliver up to a sustained 50 gigabytes per second from 8 independent 128 bit data ports on a double pumped data bus. Data burst length can be programmed to 4 or 8 words; bursts of 8 can be interrupted with no bus penalty.

The Octopus contains an on-board ECC system called Bit Armor™ that provides ECC protected data for extended error-free operation. Bit Armor requires no host device alterations or data insertion paths, thus providing a simple and highly usable method for yield enhancement.

Interface adaptation is made simple by mimicking the industry standard DDR DRAM interfaces. A wide variety of I/O and addressing options is available with either soft configuration or factory antifuse programming.

The I/O is designed for 1pf loads at a maximum data rate of one giga-transfer per second.

Block Diagrams

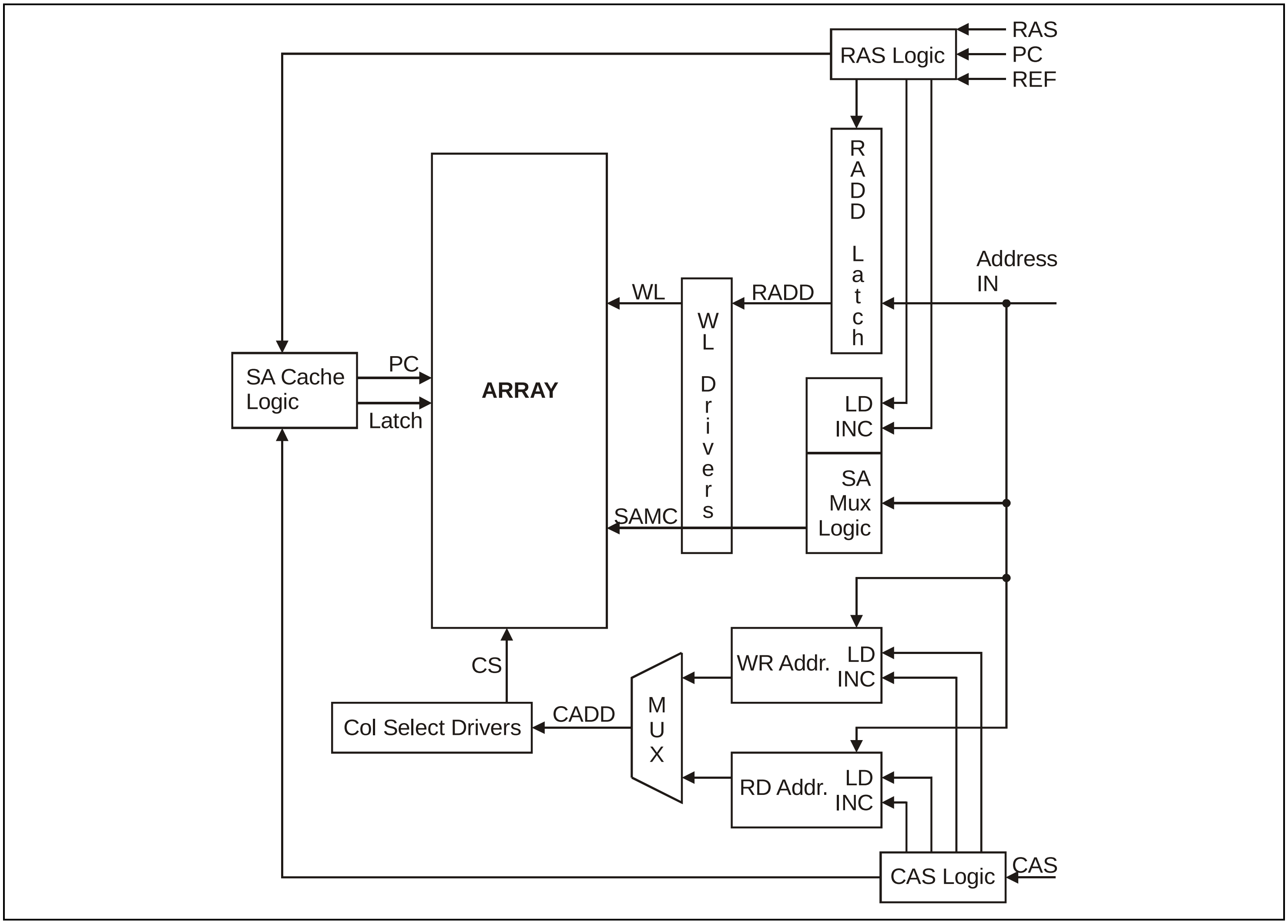

Figure 1: Simplified address path

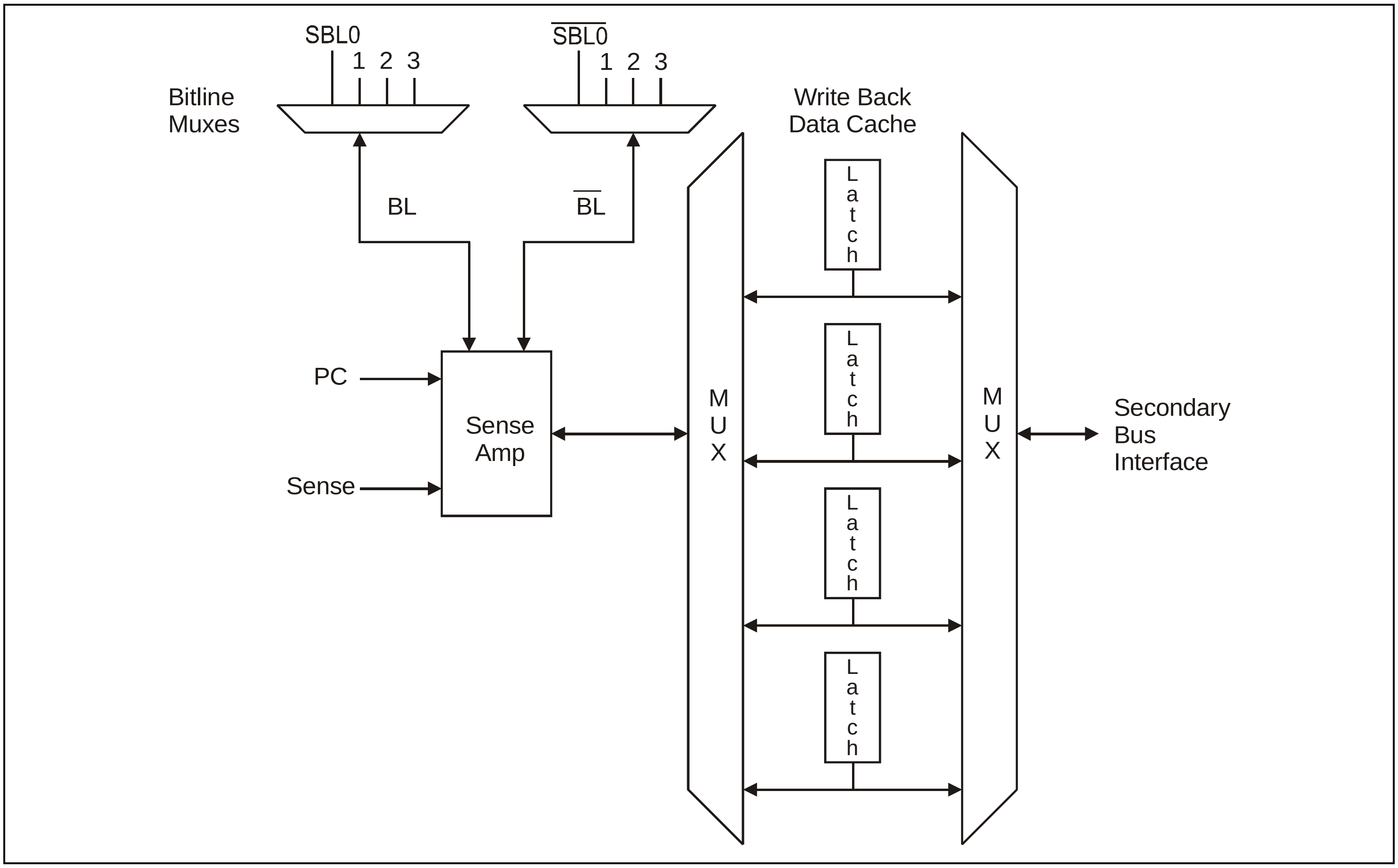

Figure 2: Sense amp logic diagram

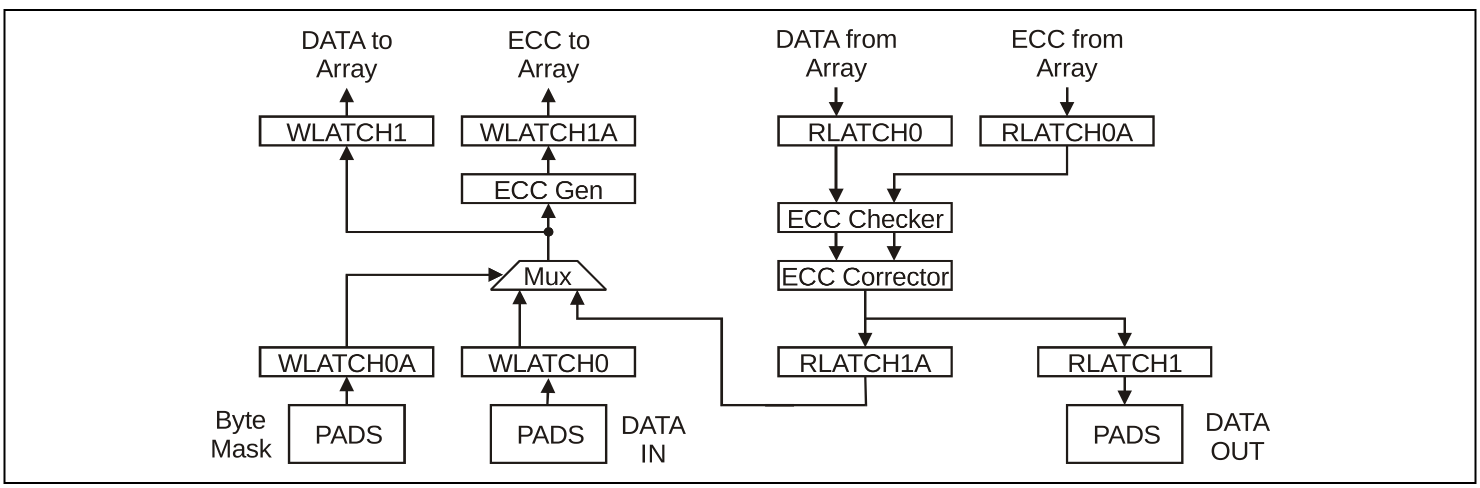

Figure 3: Simplified data path

Functional Details

General Description

The Octopus is a 3D IC designed with one controller layer and up to 4 layers of memory cells, each memory cell layer containing 1Gb of useable DRAM. It offers an 8-port configuration with 128 data bits per port in each direction for a total bus width of 1024 bits, capable of delivering a sustained 50 gigabits per second. Octopus contains a layer of optimized logic, separate from the DRAM cells, with an on-board Bit Armor™ engine for ECC.

The standard interface is logically and functionally compatible with both DDR2 and DDR3, but can be customized to suit the host device. The interface documented here has been simplified for greatest flexibility and easiest implementation. The interface can be separated into 9 subsections: 8 identical port interfaces and one common “mailbox” interface for out-of-band DRAM configuration and control.

Operational Information

On power-up, the Octopus should first be reset and then configured before use. Both reset and configuration are done through the mailbox.

The Octopus may operate in either Burst 4 mode or Burst 8 mode. The burst mode is set in a control register via the mailbox. On-the-fly changing is not supported.

The recommended operating temperature range is 0°C to 115°C. Burn-in under bias: 125°C.

Refresh rates vary from 8 to 64 ms, depending upon the operating temperature:

Table 1 Refresh Rates

Temperature	Refresh Rate
85-0°C	64 ms
85-95°C	32 ms
95-115°C	8 ms

The user is responsible for refreshing the memory at a rate sufficient to maintain the contents. If temperature is in doubt, a faster rate is safer (although it uses more power). All rows must be refreshed within the Refresh Rate interval. Individual row intervals within the Rate interval are not important. Refresh commands can be run in succession, or spaced out as desired, as long as all rows are refreshed within the Rate interval.
Note: If you wish to use only a small subset of the DRAM, the Refresh with automatic counter may not be ideal. You can manually refresh only the rows that you are using. To refresh a row manually, do a Row Address followed by a PreCharge. This takes a bit more power than a Refresh and it takes a bit longer, but the power/latency issue will be offset if you ignore many unused rows.

There are five basic memory functions: Row Address, Column Write, Column Read, Refresh, and PreCharge. The user must program the timing for RAS to CAS, PC to RAS or Ref, CAS to data in, CAS to data out, and write recovery time.

Data is always DDR.

Port Details

Each port has a 128 bit data interface with accompanying address and data access controls. There is no relationship in timing or data space between the ports. Each port accesses a separate data space and all ports can act asynchronously to one another.

Each port accesses a bank of memory that is made of two memory blocks acting in ping-pong fashion to supply data at the highest possible data rate. The capacity of each block is from 64 Mb to 256 Mb, depending on the number of memory cell layers. Each block has two 64 bit ECC circuits acting on internal odd and even data. The sense of odd and even does not have an external reference; it relates only to the internal design. Each ECC can process a 64 bit word in one clock cycle. In 128 bit wide operation, the two 64 bit ECCs act simultaneously to generate the 128 bit word. The two blocks (with a total of 4 ECC circuits) ping-pong to generate two 128 bit words each cycle. The data burst can be sustained for a maximum of 4 clocks or 8 data transfers. It is possible, depending on speed, to continuously burst within one page; however, this specification assumes a one-clock "bubble" between data bursts.

The block diagrams illustrate the basics of memory operation. Each of the latch stages may be programmed to run at a unique timing which may or may not be directly associated with an external clock edge. Latches may also be bypassed depending on the timing settings.

Each port accesses 8192 rows per cell layer, addressed with lines A12:A0. There may be as many as four layers of cells, addressed with lines A14 and A13. These layer selects are treated as additional row addresses.

Each beat of data within a burst returns 128 bits, the contents of an entire column. There are 128 columns per row, addressed with lines A6-A0. These signals specify which column to read; they do not permit a starting offset within the column.

Command Functionality

Row Address

Opens a row and reads the entire row (128 columns; 16384 bits) into a buffer. If the previous row was not closed, any data in that row (and in the buffer) is lost. This command uses address lines A14:A0.

Column Read

Reads either 4 or 8 entire columns of data (128 bits each) from the buffer to your device. This command uses address lines A6:A0. If the value of A1:A0 is 00 the read will happen more quickly.

Column Write

Writes 4 or 8 bursts of data from your device to the buffer, up to 128 bits per burst, controlled by byte mask signals.

PreCharge

Writes the entire buffer contents out to the open row and closes that row.

Refresh

Opens and closes a row. If the previous row was not closed, any data in that row (and in the buffer) is lost. Refresh maintains its own row counter.

About PreCharge and Refresh: If a row is open, PreCharge before Refresh is mandatory to prevent data loss in that row. PreCharge is never necessary after Refresh; it is supported for compatibility only.

A Special Note About PreCharge

After each Row Address (RAS) there **must** be a PreCharge (PC) to properly close the row before a Refresh (Ref) or another RAS. Without a PC, data in the open row **will be lost**.

This memory uses PreCharge (PC) differently than most DRAMs because of its 4 bit sense amp cache. This cache provides faster write in open page operation, allows the sense amp muxing to operate with minimal impact, and allows the architecture to use less power in normal operation. PC in this device actually retires the cache lines back to the open memory row.

After a Ref command, no PC is needed. If one is issued, the device will write back the data in the cache line, but this is not required.

Addressing

Regardless of burst length, an address with both A0 and A1 set to zero defines an “aligned” access; otherwise, the access is considered unaligned. It is recommended that A0 and A1 always be set to 0,0 to avoid additional CAS latency (see timing section).

If the initial address is not at a burst boundary, the columns returned will “wrap” within the burst. Examples:

Burst 4: if the two low-order address bits (A1 and A0) are not 0,0 then the four columns retrieved will "wrap" within the four. For example, starting at 3 will return 3-0-1-2.

Burst 8: if the three low-order address bits (A2, A1, and A0) are not 0,0,0 then the eight columns retrieved will "wrap" within the eight. Starting at 3 will return 3-4-5-6-7-0-1-2.

Table 2 Port Signals

Symbol	Type	Description
DI[127:0]	Input	Data In
DO[127:0]	Output	Data Out
DM[15:0]	Input	Data Mask for write, one signal per data byte; high = mask, low = write. DM has exactly the same timing as DI and is sampled exactly like data.
Clk	Input	Clock
RdClk	Output	“Read Clock” – actually a data strobe line
CS#	Input	Chip Select, active low
Ref#	Input	Refresh, active low
CAS#	Input	Column Access “Strobe”, active low
RAS#	Input	Row Access “Strobe”, active low
PC#	Input	PreCharge, active low
WE#	Input	Write Enable, active low
A[14:0]	Input	Address, multiplexed bus

All signals are 1.5V rail-to-rail CMOS compatible.

All signals should be assumed to be 25ff , except that Clk will have a capacitance of 125ff.

Port Timing

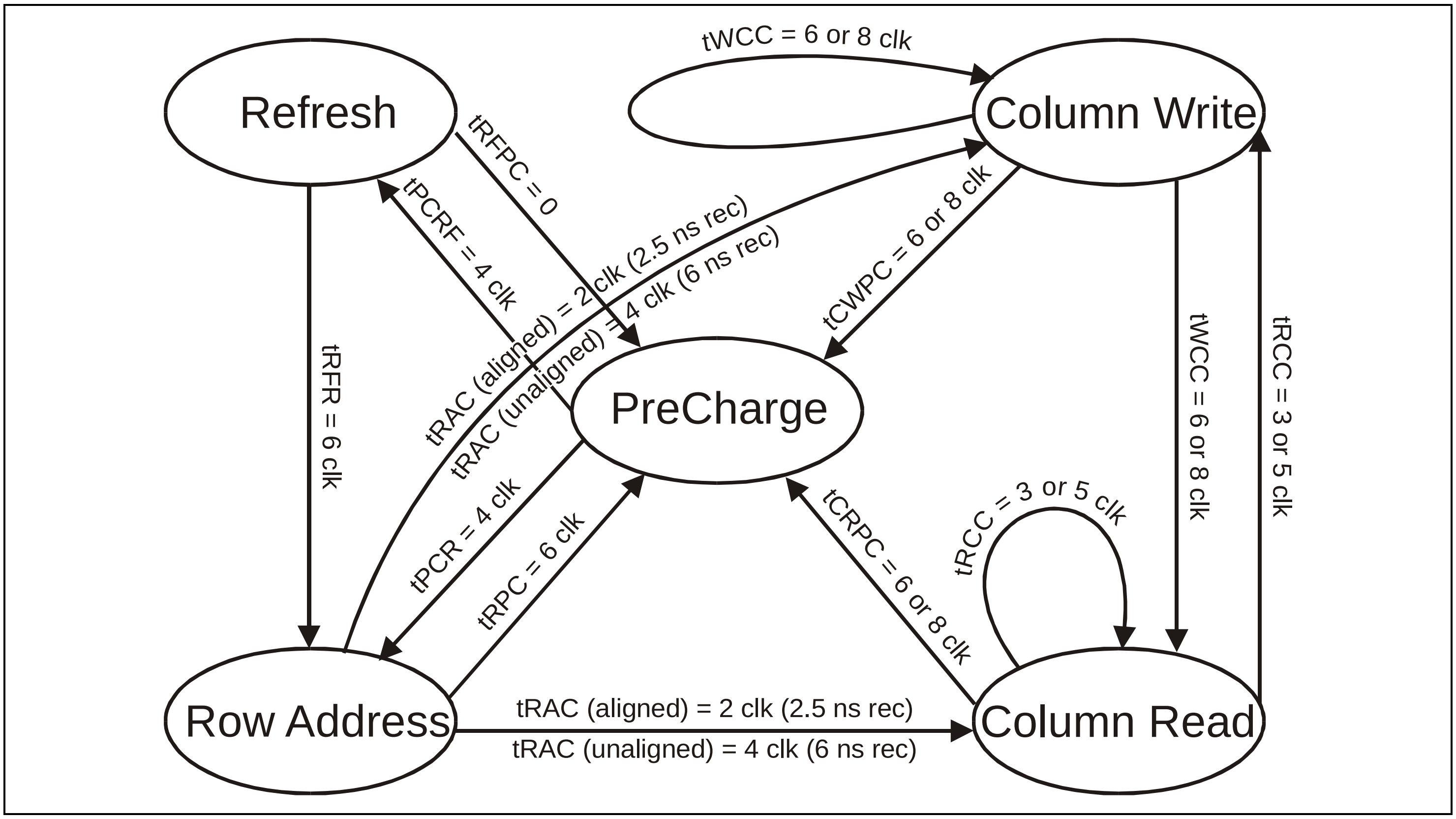

Figure 4: State Diagram

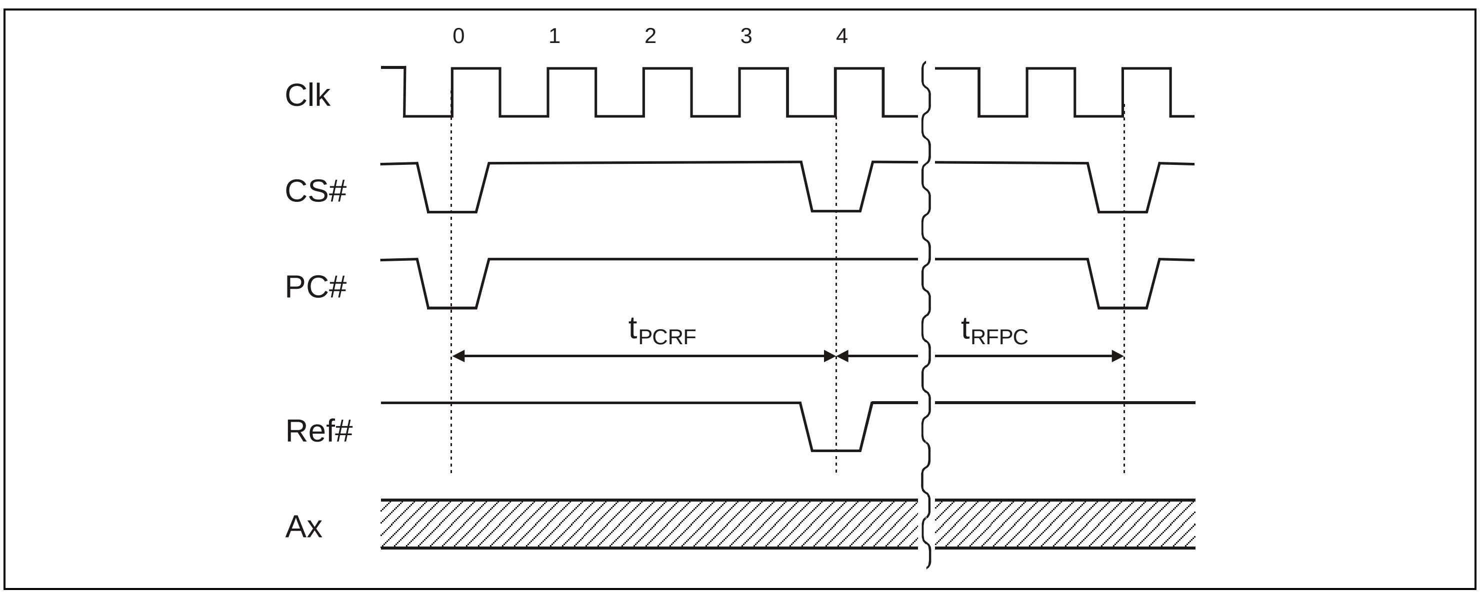

Figure 5: Refresh

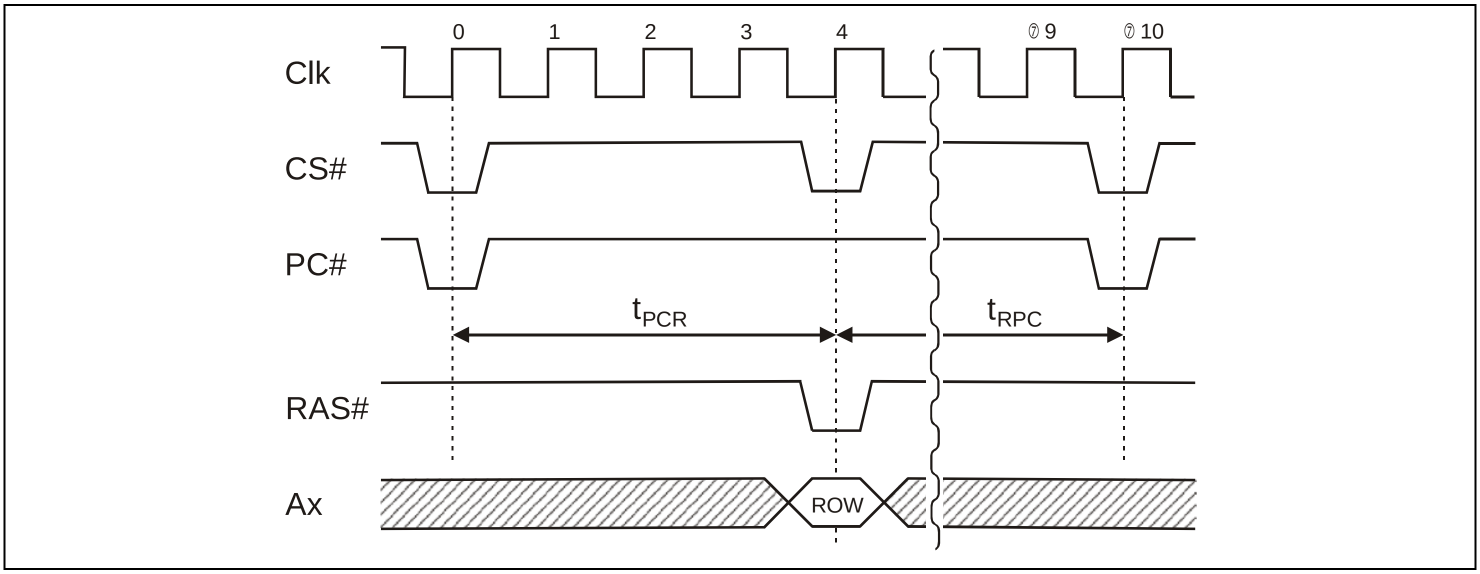

Figure 6: Row Access

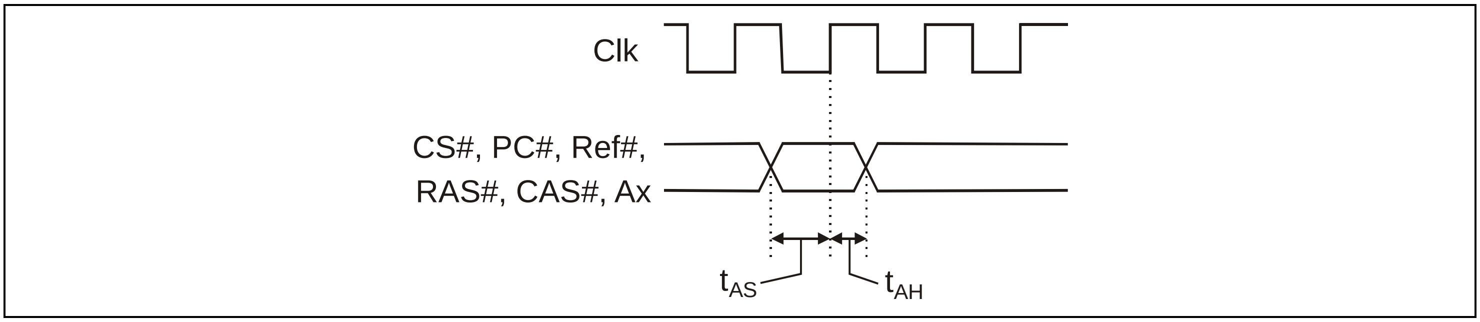

Figure 7: Address/Command Setup and Hold

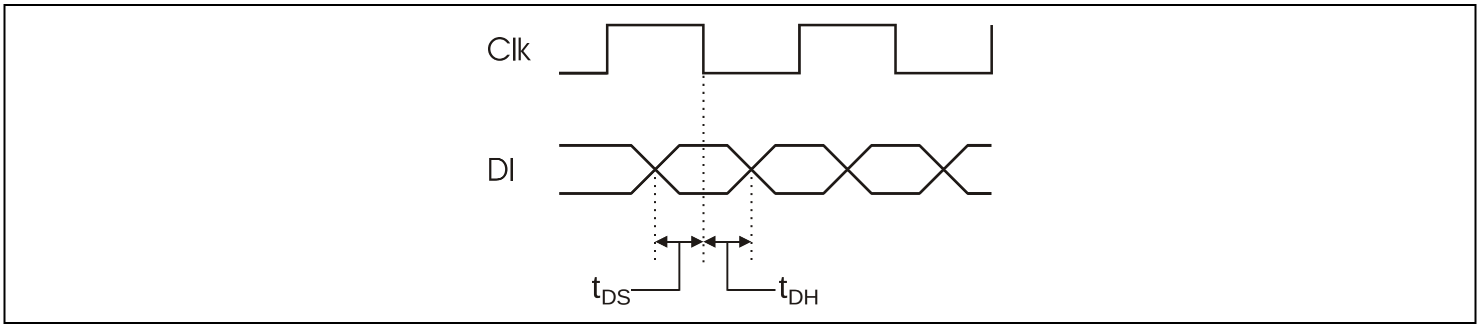

Figure 8: Input Data Setup and Hold

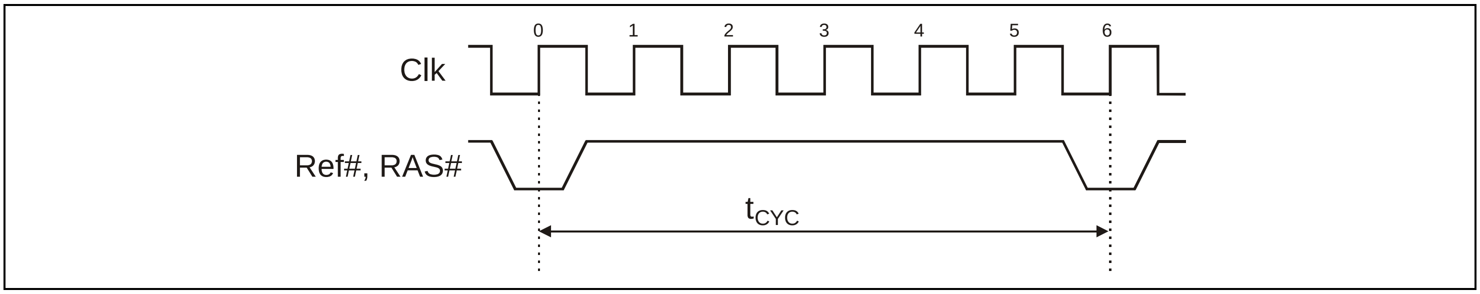

Figure 9: Memory Cycle Time

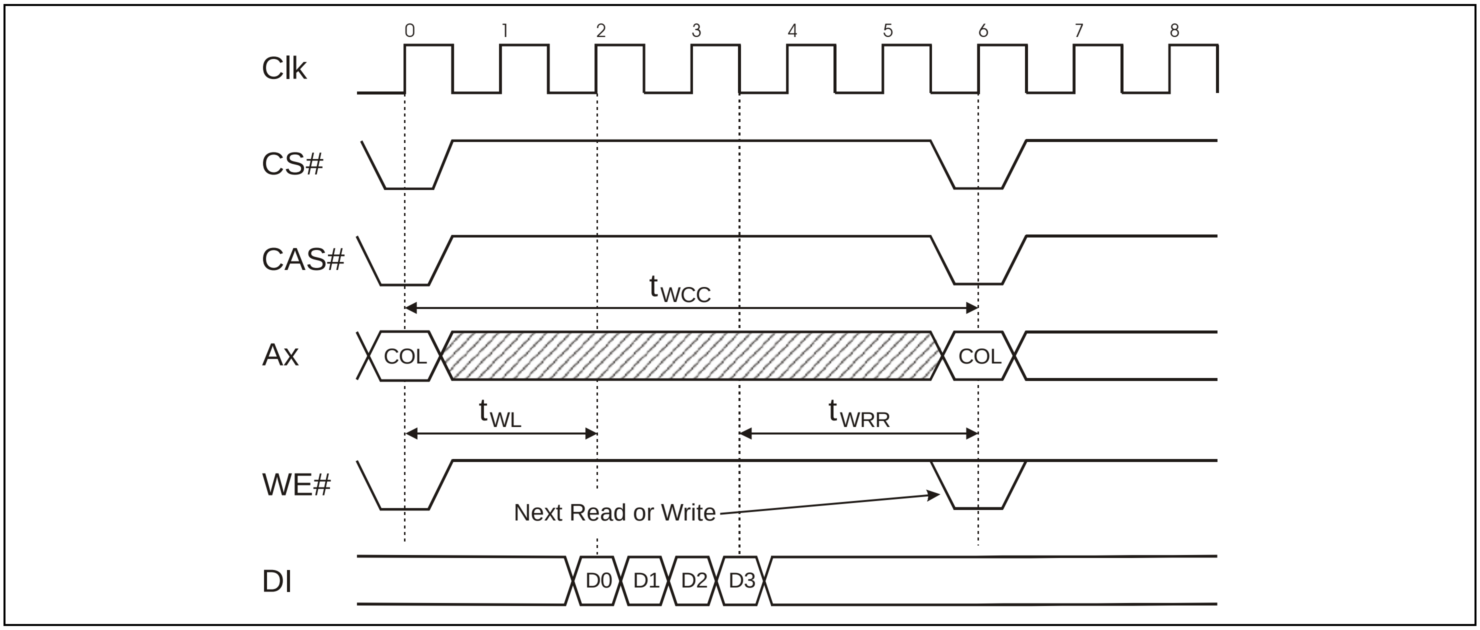

Figure 10: Burst 4 Write, WL=2

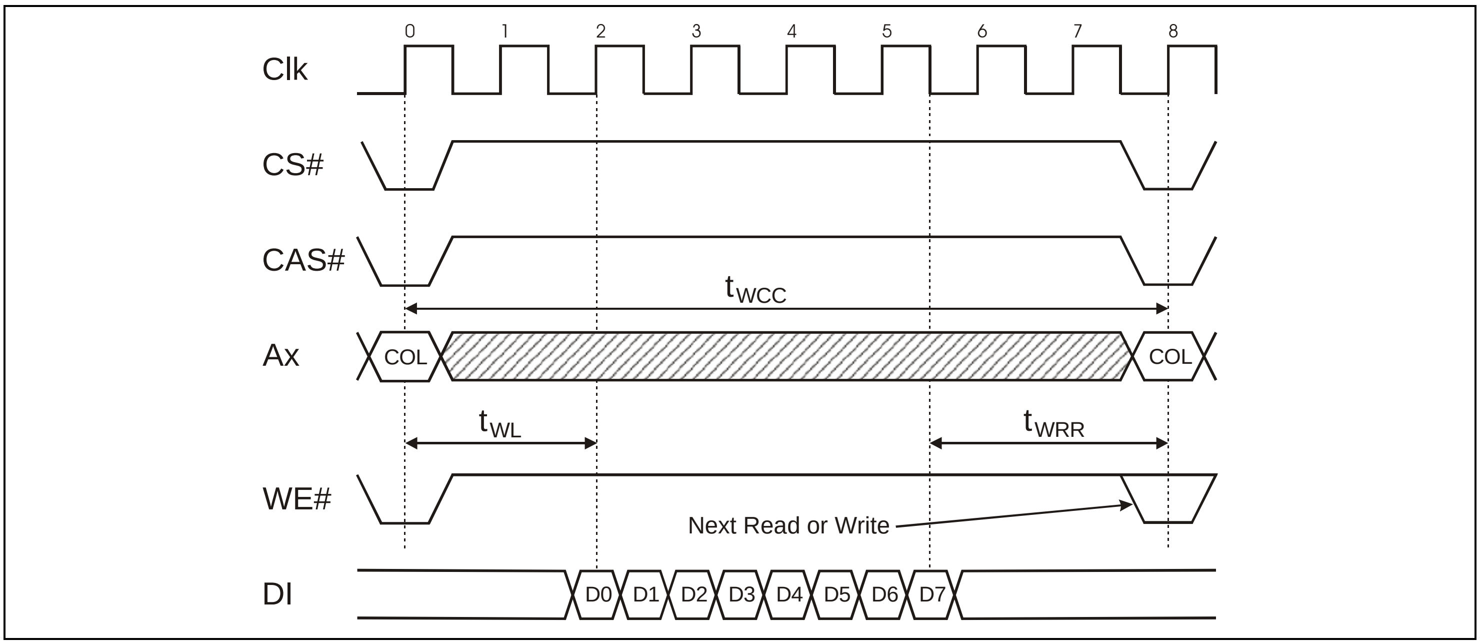

Figure 11: Burst 8 Write, WL=2

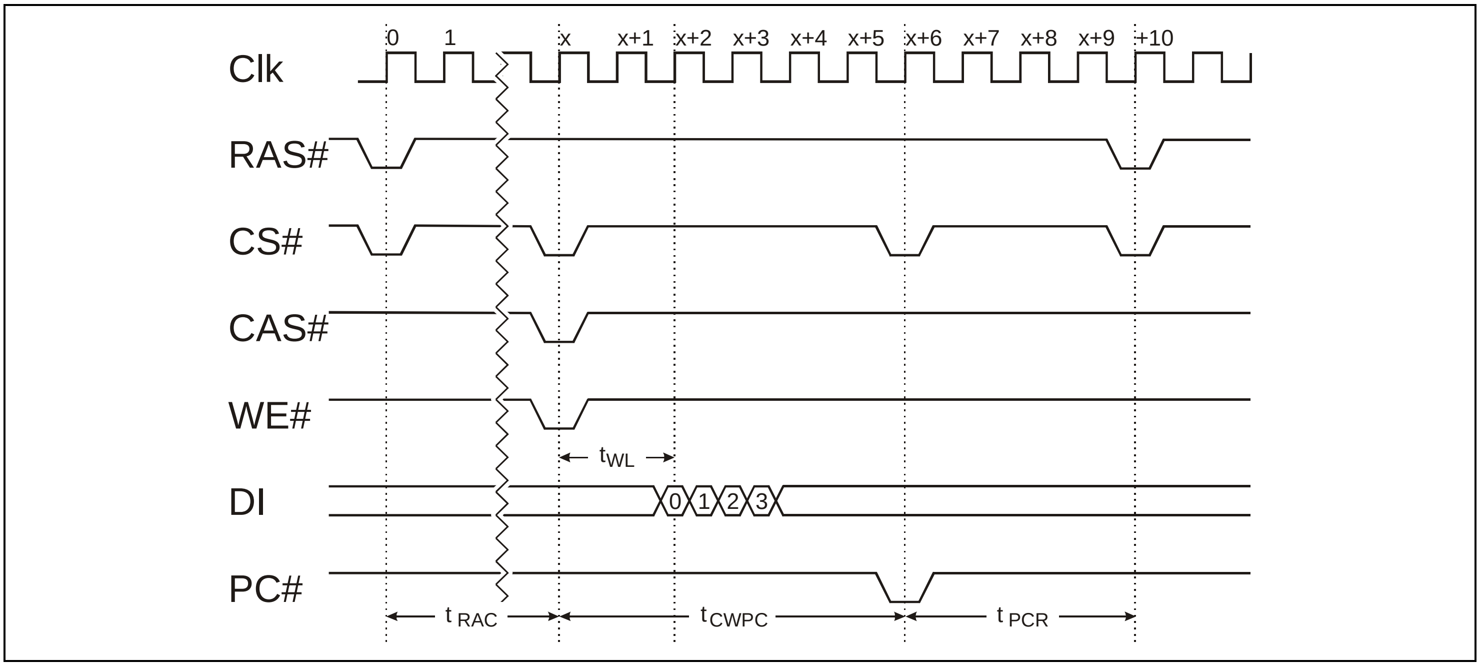

Figure 12: Burst 4 Write, WL=2, with PreCharge and Row Activate

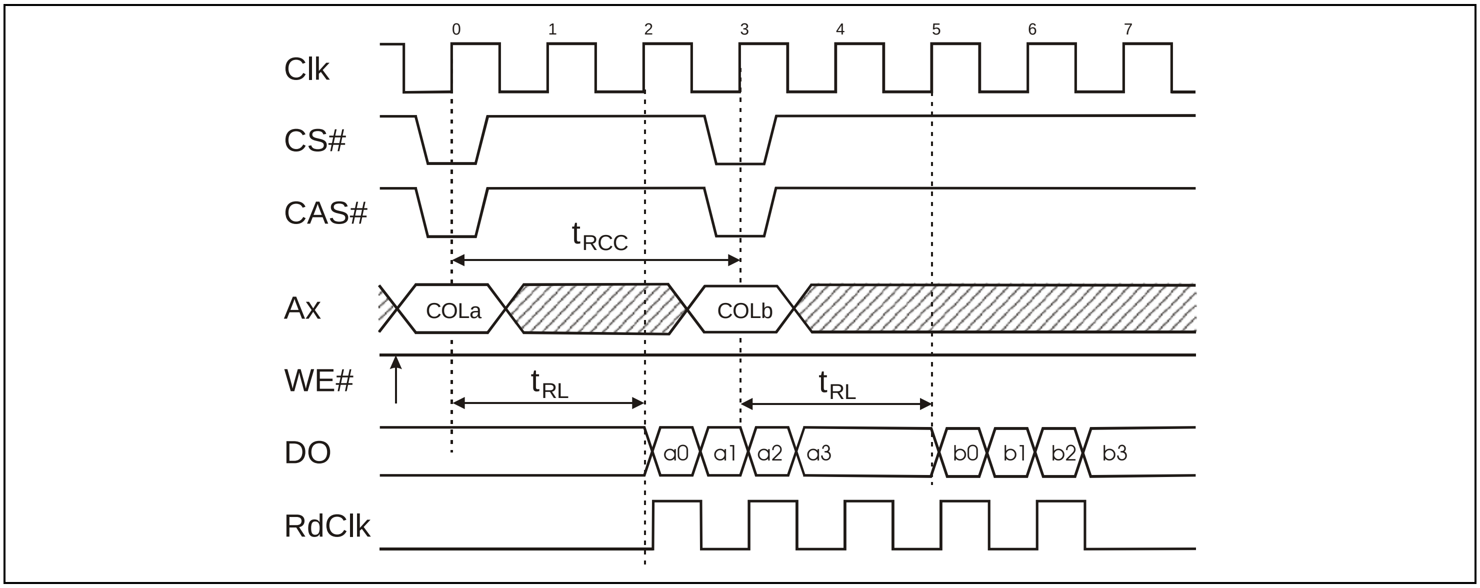

Figure 13: Burst 4 Read, RL=2 (two consecutive operations)

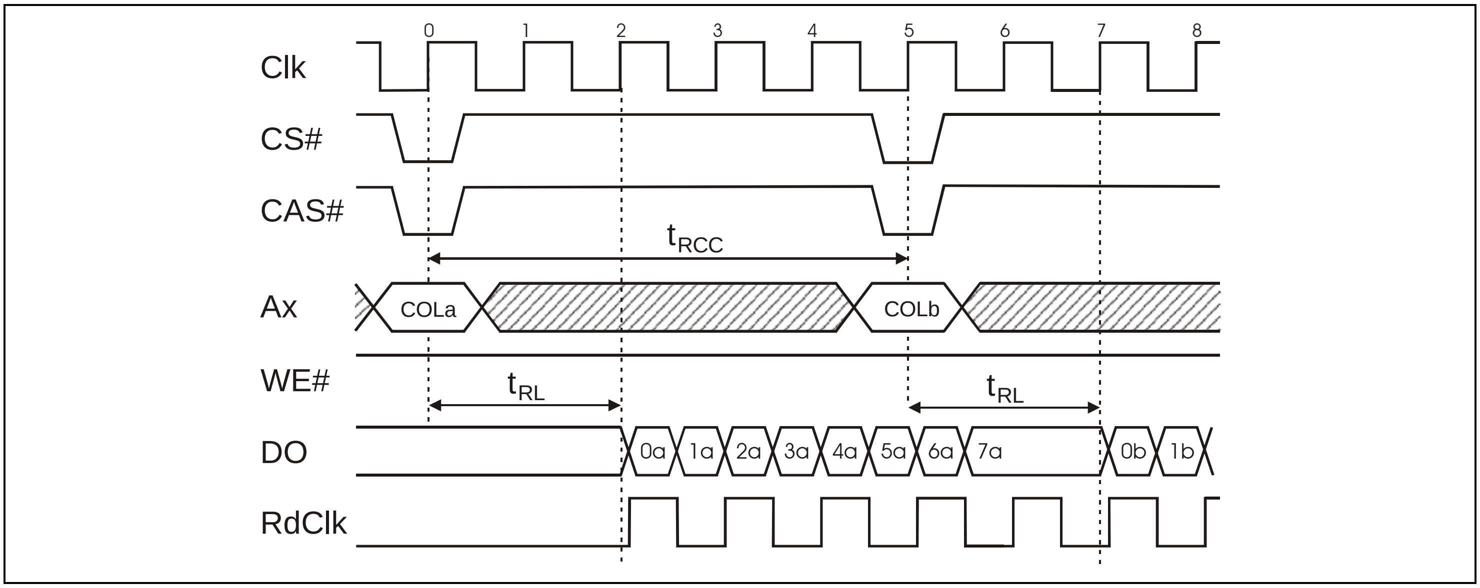

Figure 14: Burst 8 Read, RL=2 (two consecutive operations)

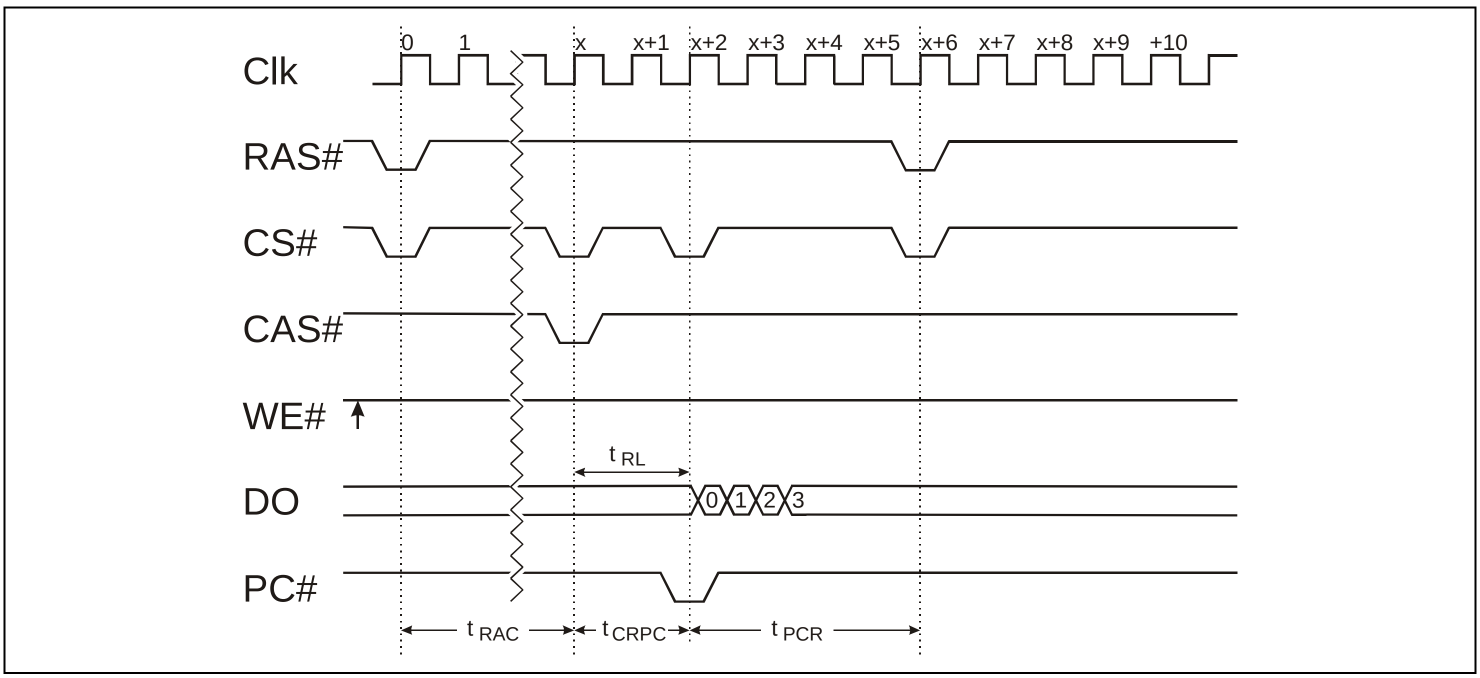

Figure 15: Burst 4 Read, RL=2, with PreCharge and Row Activate

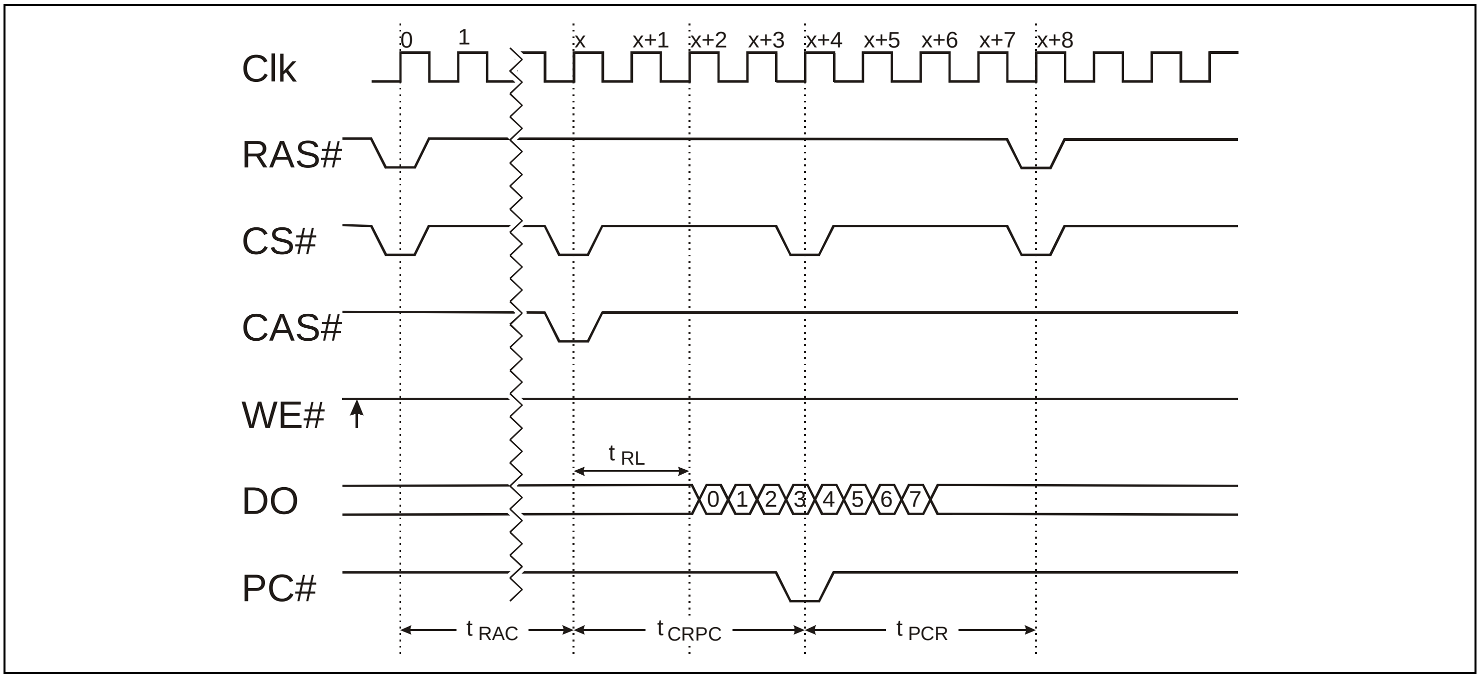

Figure 16: Burst 8 Read, RL=2, with PreCharge and Row Activate

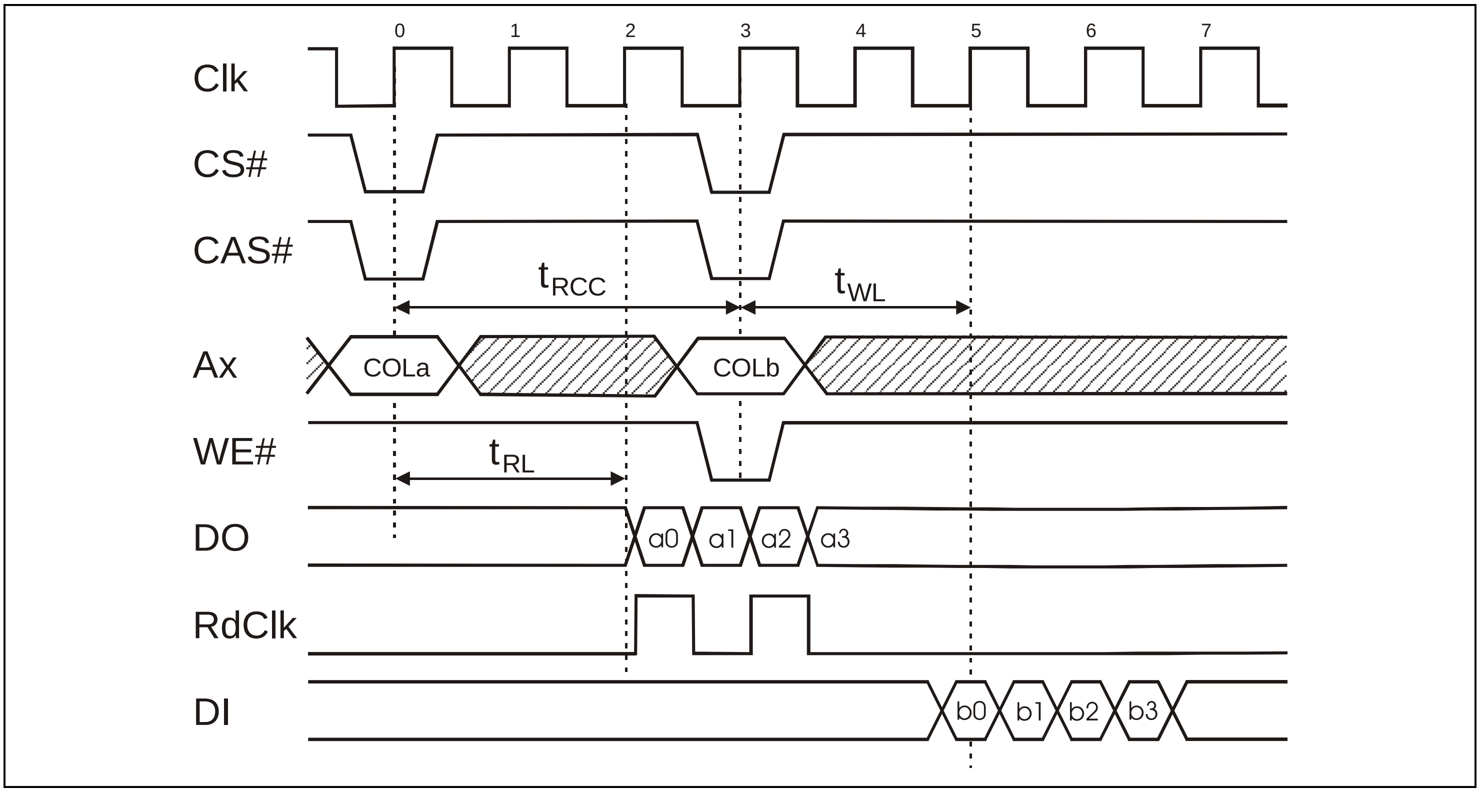

Figure 17: Burst 4 Read-to-Write (same row), RL=2, WL=2

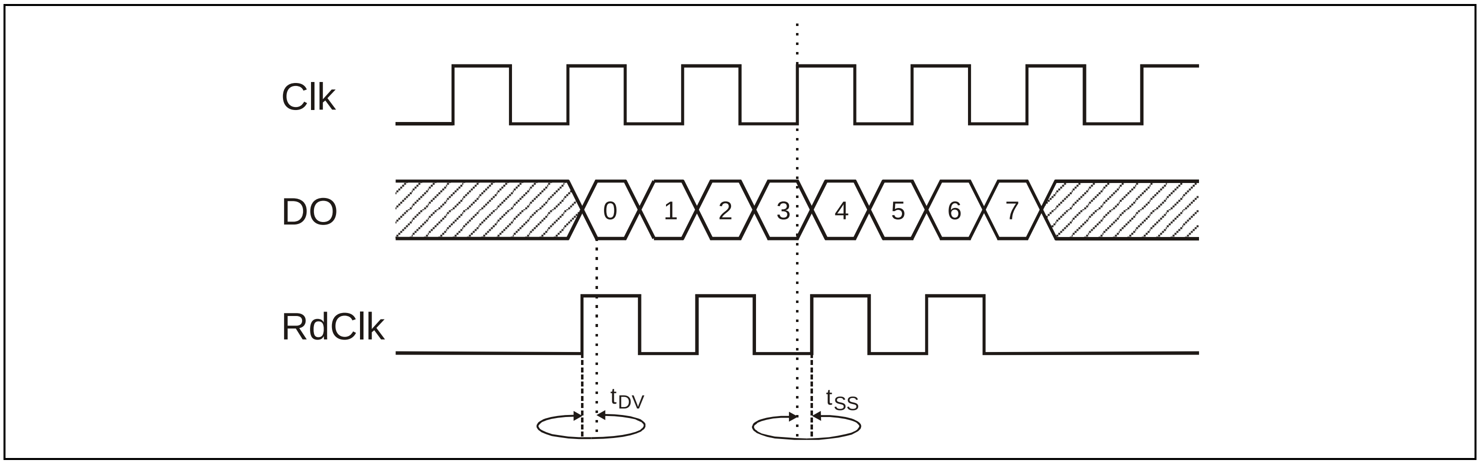

Figure 18: RdClk and Read Data Skew

Table 3 Memory port timing

Name	Description	Minimum	Maximum	Recommended
tDS	Data setup	250 ps		300 ps
tDH	Data hold	100 ps		150 ps
tAS	Address/Command setup	250 ps		300 ps
tAH	Address/Command hold	250 ps		300 ps
tCYC	Memory cycle time; Ref or RAS to next Ref or RAS	6 clks		7.5 ns
tRAC	RAS to CAS aligned access (two least significant address bits are 00)	2 clks		2.5 ns
tRAC	RAS to CAS unaligned access (two least significant address bits not 00)	4 clks		6 ns
tRCC	Read CAS to next CAS (any)	BC+1 clk		
tWCC	Write CAS to next CAS (any)	BC+tWL+tWRR		
tCWPC	CAS Write to PC	BC+tWL+2 clks		
tCRPC	CAS Read to PC	BC+tRL–2 clks		
tWL	CAS Write latency	2 clks		
tRL	CAS Read latency	2 clks		
tSS	RdClk skew from Clk		350 ps	
tDV	Valid data alignment; the time between RdClk high and data valid.		• 125 ps	
tRPC	RAS to PC	6 clks		
tPCR	PC to RAS	4 clks		4 clks, 5 ns
tPCRF	PC to Ref	4 clks		4 clks, 5 ns
tRFPC	Ref to PC	0 clks		0 clks
tRFR	Ref to RAS	6 clks		
tWRR	Write recovery	2 clks		
tSW	Strobe width; the width of RD, WR, UAL, MAL, LAL	1 ns		
	Clk frequency		800 MHz	500 MHz
	Clk duty cycle	40%	60%	

Note: BC = data burst length, in clock cycles (2 or 4)

Timing Notes:

When accessing memory, a single row may be held open indefinitely. The only requirement for closing and re-opening a row is the Refresh rate. When issuing a Refresh, if there is an open row you must issue a PreCharge to close that row. After the Refresh, you can re-open the row with a RAS.

In consecutive Reads, assume one clock of “bubble” in the data. The memory may actually work fast enough to eliminate the bubble, but that is not guaranteed at present.

The memory does not have a lower frequency limit except for performing REFRESH.

Some timing values are given in both ns and clocks; in this case both must be satisfied. All port signal timing is synchronous to the rising or falling clock edge.

Mailbox Details

The common “mailbox” interface allows the user to access the control and settings of the DRAM. As such all DRAM control programming is out of band. There are three current items that must be set for DRAM operation. These are:

Write Latency, WL: 2 to 9

Read Latency, RL: 2 to 9

Burst length, BL: 4 or 8

Additional user controls may be specified in the future.

Mailbox Operations

Reset

Reset is required before using the memory. Assert the Reset signal for at least 1 ns. After Reset, wait at least 100 ms before any other operation.

Write

The mailbox uses 24bit addresses written in three 8bit pieces. They may be written in any order. The timing diagrams use the order UAL, MAL, LAL. The address latch values are retained from one mailbox transaction to the next so only the address bytes that change need to be written from one cycle to the next. Reads and writes share the same physical address registers. A write is committed with the rising edge of the WR strobe. The data written is that which is present on the data bus input at the time of the rising WR strobe edge.

Read

The mailbox read addressing follows the exact same method and timing as used for writing the mailbox. The read operation is triggered with the rising edge of the RD strobe. When the read data is available on the DO[7:0] signal pins, the Ready signal will toggle high for one AuxClk period. The data will be latched at the DO pins on the falling edge prior to the Ready signal toggling high. The data will remain valid until the next rising edge of the RD strobe.

Bypass

This function uses the same timing as other mailbox functions. It allows direct access to everything in the memory. Internal memory addresses have not yet been released.

Table 4 Mailbox registers

Name	Address	Data byte
RL	00 00 00 00h	0Ah = 2, 0Bh = 3, 00h = 4, 01h = 5, 02h = 6, 03h = 7, 04h = 8, 05h = 9
WL	00 00 00 01h	
BL	00 00 00 03h	02h = BL4, 00h = BL8

Table 5 Mailbox signals

Name	Direction	Description
MDI[7:0]	Input	Mailbox Data In
MDO[7:0]	Output	Mailbox Data Out
AuxClk	Input	Mailbox host side state machine clock.
UAL	Input	Upper Address Latch, active high
MAL	Input	Middle Address Latch, active high
LAL	Input	Lower Address Latch, active high
Ready	Output	Output data is ready, active high
WR	Input	Data Write, active high
RD	Input	Data Read start, active high
Reset	Input	Resets the entire memory device, active high; all data is lost. After reset the memory is unavailable for ~100 ms for initialization. Reset is required before the first memory operation (port or mailbox).
Bypass	Input	Active high. This isolates the on-board memory CPU. The mailbox then has unfettered access to the entire memory configuration bus including the RAM, ROM, PROM, and all control registers.

Mailbox Timing

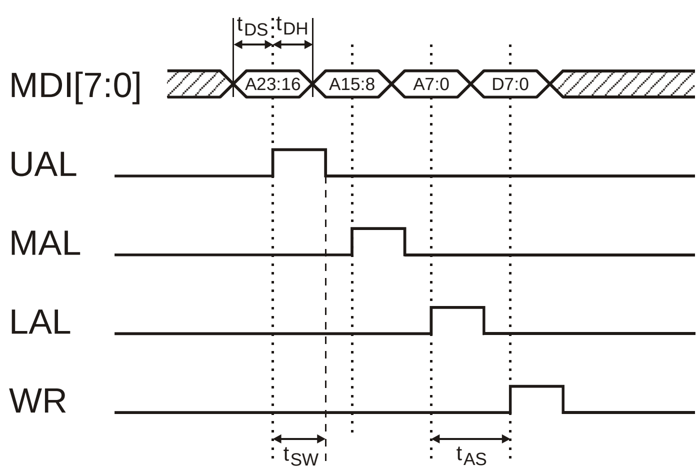

Figure 19: Mailbox Write

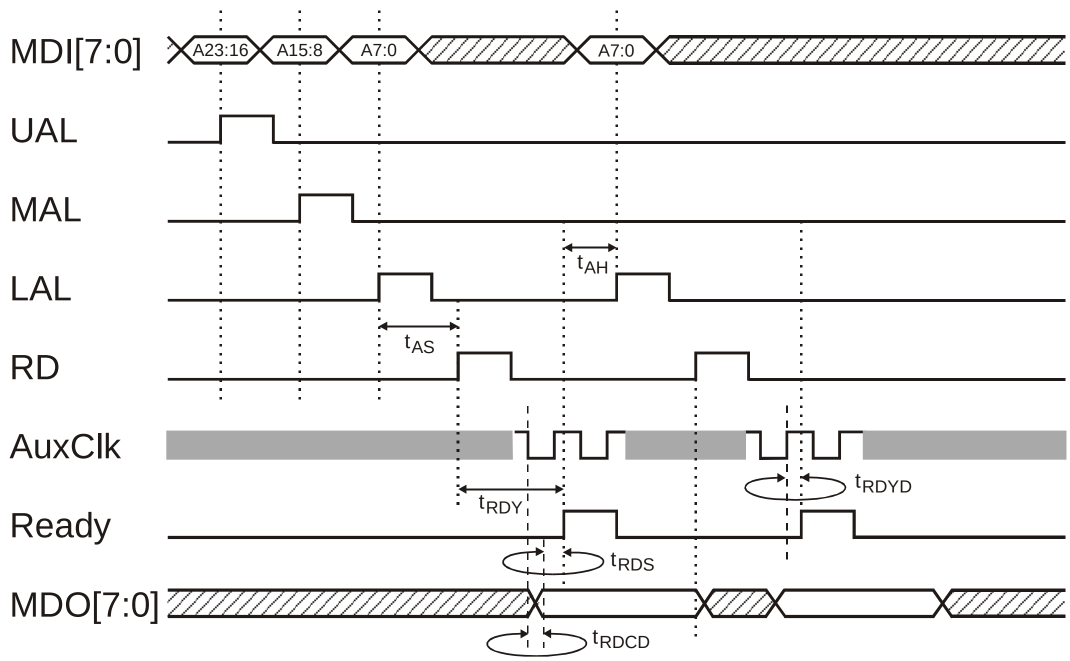

Figure 20: Mailbox Read

Table 6 Mailbox timing

Symbol	Description	Min	Max	Recommended
tDS	Data setup to UAL, MAL, LAL, WR	250ps		
tDH	Data hold for UAL, MAL, LAL, WR	100ps		
tRDY	RD to Ready High		10 ns	
tAS	Setup for UAL, MAL, LAL to UAL, MAL, LAL, WR, RD	1 ns*		
tAH	Time from Ready to address byte	250 ps		
tWRR	WR to UAL, MAL, LAL, WR	10 ns*		
tRSTR	Reset negate to first memory access or configuration programming	100 ms		
tRDCD	Read data delay		500 ps	
	AuxClk frequency		200 MHz	
	AuxClk high time	1 ns		
	AuxClk low time	1 ns		
tRDS	Read data setup	500 ps		
tRDH	Read data hold	0		
tRDYD	Ready skew from AuxClk		500 ps	
	Ready pulse width = AuxClk cycle			

*** tAS and tWRR for the Mailbox are NOT the same as tAS and tWRR for the DRAM itself**

Characteristics

Table 7 Absolute Maximum Ratings

Symbol	Description	Value	Unit
Vdd	Core voltage	1.9	V
Vddq	I/O voltage	1.9	V
Vss	Ground	–0.4	V

Table 8 Power Supply Voltage

Symbol	Min.	Typ.	Max.	Unit
Vdd	1.4	1.5	1.7	V
Vddq	1.4	1.5	1.7	V

Table 9 Logic Voltage

Condition	Symbol	Min.	Typ.	Max.	Unit
@ ±10µA	Vih	1.1	1.5	1.7	V
@ ±10µA	Vil	– 0.2	0.0	0.4	V
@ –50µA	Voh	Vdd-0.2			V
@ 50µA	Vol			Vss+0.2	V

Table 10 Package Dimensions

Symbol	Description	Min	Nom	Max
	Length		21.8 mm	
	Width		12.3 mm	

Physical Drawings

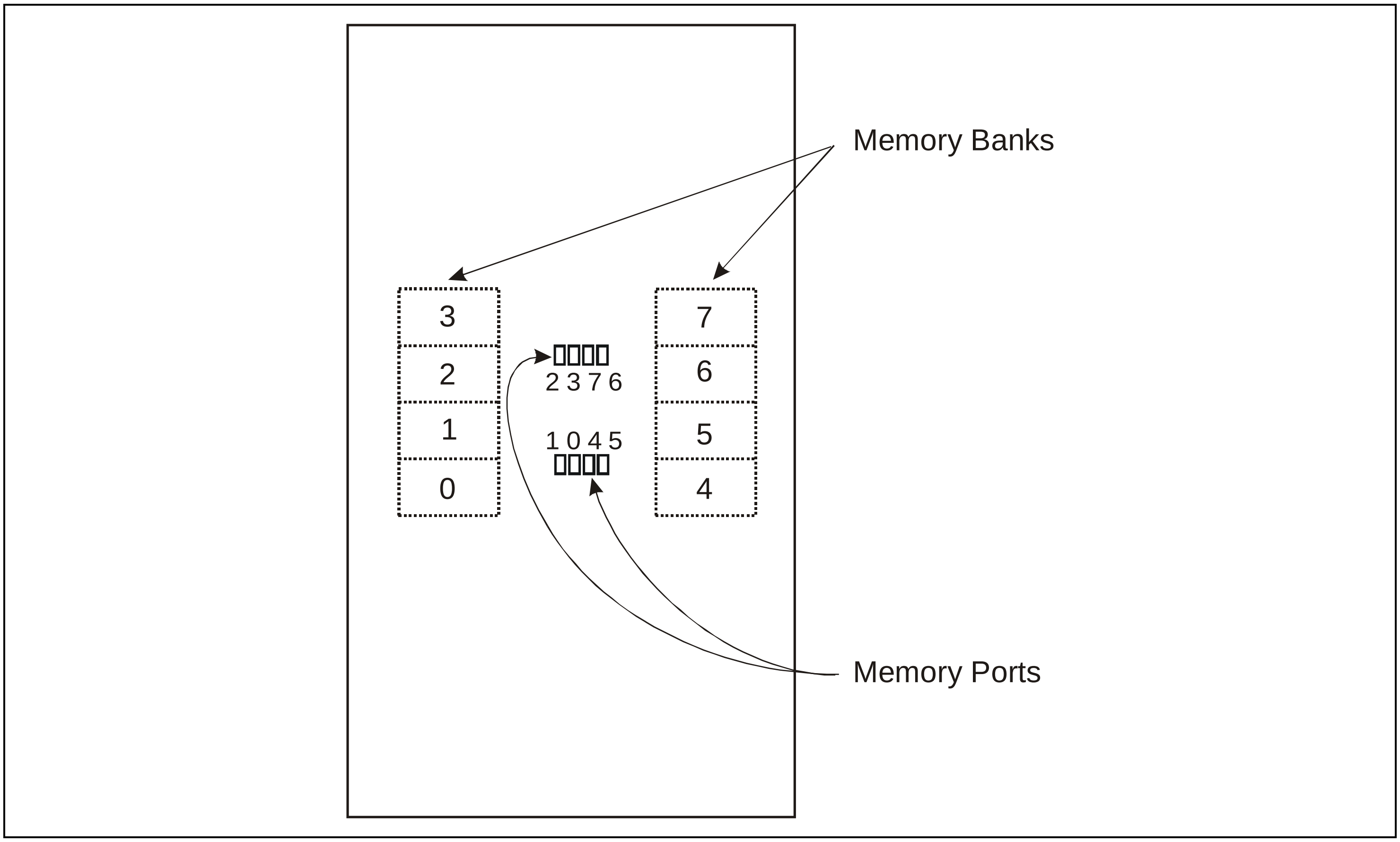

Figure 21: Placement of Ports and Memory Banks

Note: Complete pinouts and exact position information available upon request, given in .gds format.

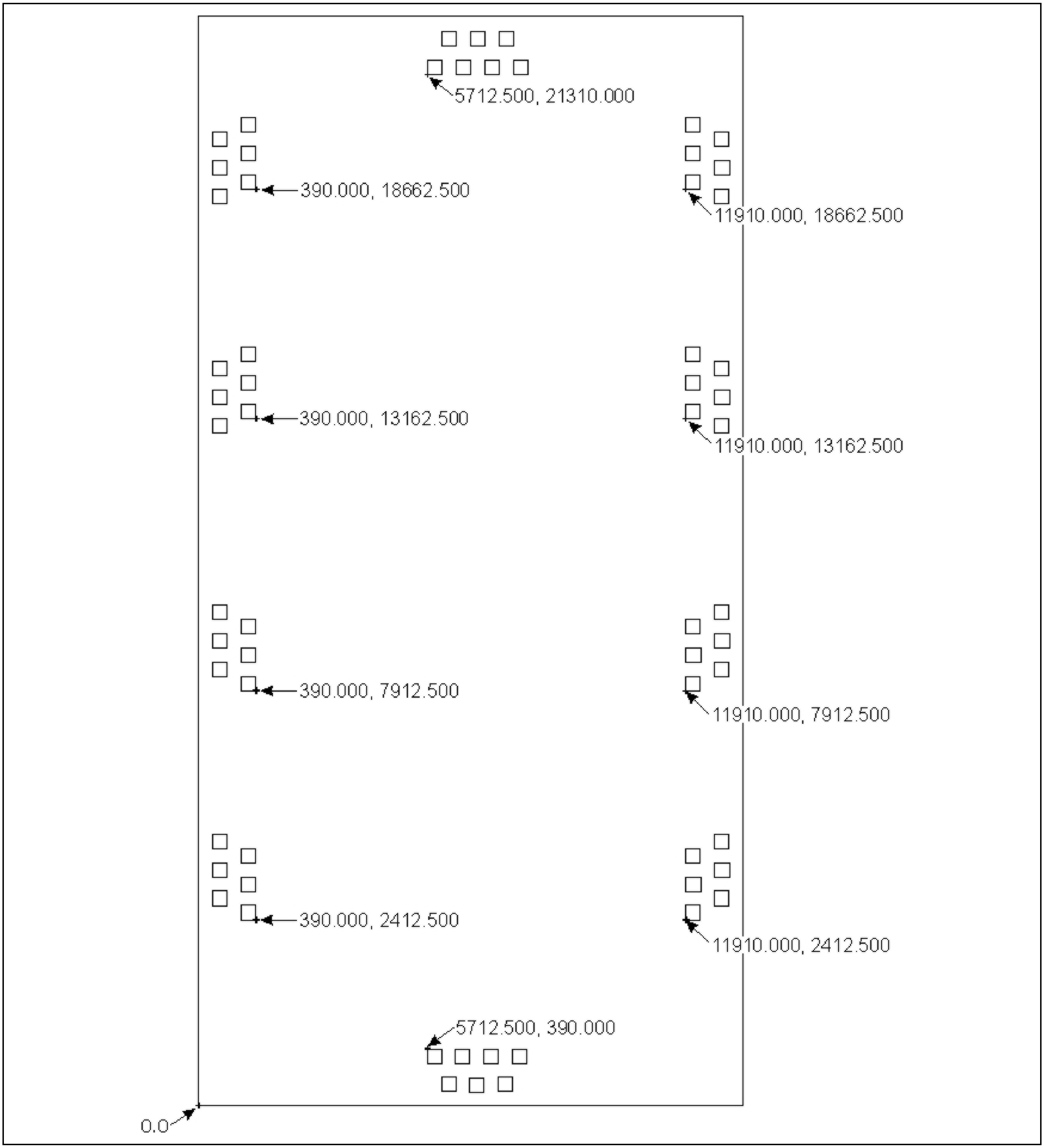

Figure 22: Placement of VDD and VSS pads

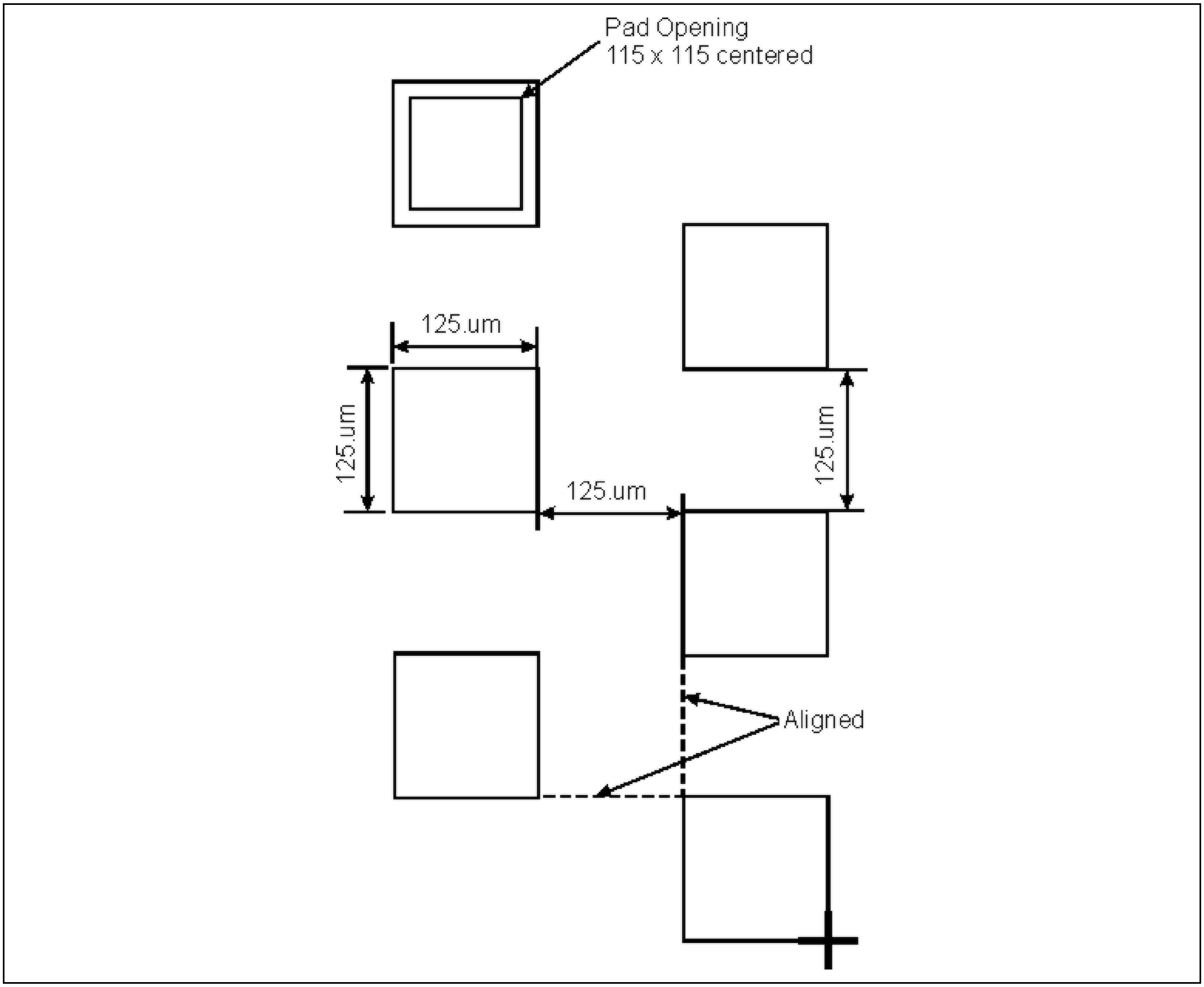

Figure 23: Close-up of VDD and VSS pads

Document History

Datasheet for TSC100801/2/4

Revision Number	Date	Changes
0.1	May 04, 2010	Original

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