72 Mb Synchronous NBT 3T-iRAM™

Pipelined, SRAM-Compatible

Features

- Error-resistant 3T-iRAM™ technology
- NBT (No Bus Turnaround) functionality for zero wait Read-Write-Read bus usage
- Fully pin-compatible with pipelined NtRAM™, NoBL™ and ZBT™
- 2.5 V ±10% core power supply, 1.8 V or 2.5 V I/O supply
- LODRV pin for user-selectable drive strength
- IEEE 1149.1 JTAG-compatible Boundary Scan
- $\overline{LBO}$ pin for Linear or Interleaved Burst mode
- Pin-compatible with 2/4/9/18/36Mb devices
- Byte write operation (9-bit Bytes)
- 3 Chip Enable signals for easy depth expansion
- ZZ pin for automatic power-down
- JEDEC standard 119- and 165-FBGA packages

Options / Marking

▪ Configurations:	4M x 18	TSC2L72T18
	2M x 36	TSC2L72T36
▪ Packages:	119-FBGA	A
	165-FBGA	B
▪ Speed (MHz):	250	-250
	200	-200
	166	-166

Part number example: **TSC2L72T36A-200**

Functional Description

3T-iRAM™ is a unique type of dynamic memory. Tezzaron has crafted these pseudostatic devices to provide entirely SRAM-compatible interfaces and timing. The unique design of these 3T memories provides soft error rates up to 10 times lower than equivalent high-speed, high-density SRAMs.

The TSC2L72T18/36 is a 72Mbit synchronous memory device that functions much like ZBT, NtRAM, NoBL, and other pipelined read/double late write SRAMs – it exploits all available bus bandwidth by eliminating “deselect cycles” when the device is switched from read to write.

As in all synchronous devices, address, data inputs, and read/write control inputs are captured on the rising clock edge. Burst order control ($\overline{LBO}$) must be tied to a power rail for proper operation. Asynchronous inputs include the Sleep mode enable (ZZ) and Output Enable ($\overline{G}$). Output Enable can override the synchronous control of the output drivers to turn them off at any time. Write cycles are internally self-timed and initiated by the rising clock edge; this eliminates the complex off-chip write pulse generation required by asynchronous SRAMs and simplifies input signal timing.

The TSC2L72T18/36 is pipelined, with a rising-edge-triggered output register. For read cycles, output data is stored in the edge-triggered output register during the access cycle and then released to the output drivers at the next rising clock edge.

Parameter Synopsis:

		-250	-200	-166	Unit
	tKQ	2.5	3.0	3.5	ns
3-1-1-1	tCycle	4.0	5.0	6.0	ns
	Curr	tbd	tbd	tbd	mA

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165-FBGA: Top View

x36 Common I/O:

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	A	$\overline{E1}$	$\overline{BC}$	$\overline{BB}$	$\overline{E3}$	$\overline{CKE}$	ADV	A	A	NC	A
B	NC	A	E2	$\overline{BD}$	$\overline{BA}$	CK	$\overline{W}$	$\overline{G}$	A	A	NC	B
C	*DQPC*	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	*DQPB*	C
D	DQC	DQC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQB	DQB	D
E	DQC	DQC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQB	DQB	E
F	DQC	DQC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQB	DQB	F
G	DQC	DQC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQB	DQB	G
H	NC	MCH	NC	VDD	VSS	VSS	VSS	VDD	NC	LODRV	ZZ	H
J	DQD	DQD	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQA	DQA	J
K	DQD	DQD	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQA	DQA	K
L	DQD	DQD	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQA	DQA	L
M	DQD	DQD	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQA	DQA	M
N	*DQPD*	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	*DQPA*	N
P	NC	A	A	A	TDI	A1	TDO	A	A	A	NC	P
R	$\overline{LBO}$	A	A	A	TMS	A0	TCK	A	A	A	A	R

x18 Common I/O:

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	A	$\overline{E1}$	$\overline{BB}$	NC	$\overline{E3}$	$\overline{CKE}$	ADV	A	A	A	A
B	NC	A	E2	NC	$\overline{BA}$	CK	$\overline{W}$	$\overline{G}$	A	A	NC	B
C	NC	NC	DDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	*DQPA*	C
D	NC	DQB	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQA	D
E	NC	DQB	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQA	E
F	NC	DQB	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQA	F
G	NC	DQB	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQA	G
H	NC	MCH	NC	VDD	VSS	VSS	VSS	VDD	NC	LODRV	ZZ	H
J	DQB	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQA	NC	J
K	DQB	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQA	NC	K
L	DQB	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQA	NC	L
M	DQB	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQA	NC	M
N	*DQPB*	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	NC	N
P	NC	A	A	A	TDI	A1	TDO	A	A	A	NC	P
R	$\overline{LBO}$	A	A	A	TMS	A0	TCK	A	A	A	A	R

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119-FBGA: Top View

x36 Common I/O:

	1	2	3	4	5	6	7	
A	VDDQ	A	A	A	A	A	VDDQ	A
B	NC	E2	A	ADV	A	$\overline{E3}$	NC	B
C	NC	A	A	VDD	A	A	NC	C
D	DQC	*DQPC*	VSS	LODRV	VSS	*DQPB*	DQB	D
E	DQC	DQC	VSS	$\overline{E1}$	VSS	DQB	DQB	E
F	VDDQ	DQC	VSS	$\overline{G}$	VSS	DQB	VDDQ	F
G	DQC	DQC	$\overline{BC}$	A	$\overline{BB}$	DQB	DQB	G
H	DQC	DQC	VSS	$\overline{W}$	VSS	DQB	DQB	H
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ	J
K	DQD	DQD	VSS	CK	VSS	DQA	DQA	K
L	DQD	DQD	$\overline{BD}$	NC	$\overline{BA}$	DQA	DQA	L
M	VDDQ	DQD	VSS	$\overline{CKE}$	VSS	DQA	VDDQ	M
N	DQD	DQD	VSS	A1	VSS	DQA	DQA	N
P	DQD	*DQPD*	VSS	A0	VSS	*DQPA*	DQA	P
R	NC	A	$\overline{LBO}$	DD	NC	A	NC	R
T	NC	A	A	A	A	A	ZZ	T
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ	U

x18 Common I/O:

	1	2	3	4	5	6	7	
A	VDDQ	A	A	A	A	A	VDDQ	A
B	NC	E2	A	ADV	A	$\overline{E3}$	NC	B
C	NC	A	A	VDD	A	A	NC	C
D	DQB	NC	VSS	LODRV	VSS	*DQPA*	NC	D
E	NC	DQB	SS	$\overline{E1}$	VSS	NC	DQA	E
F	VDDQ	NC	VSS	$\overline{G}$	VSS	DQA	VDDQ	F
G	NC	DQB	$\overline{BB}$	A	NC	NC	DQA	G
H	DQB	NC	VSS	$\overline{W}$	VSS	DQA	NC	H
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ	J
K	NC	DQB	SS	CK	VSS	NC	DQA	K
L	DQB	NC	NC	NC	$\overline{BA}$	DQA	NC	L
M	VDDQ	DQB	VSS	$\overline{CKE}$	VSS	NC	VDDQ	M
N	DQB	NC	VSS	A1	VSS	DQA	NC	N
P	NC	*DQPB*	VSS	A0	VSS	NC	DQA	P
R	NC	A	$\overline{LBO}$	DD	NC	A	NC	R
T	A	A	A	A	A	A	ZZ	T
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ	U

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Pin Descriptions

Symbol	Type	Description
A_0, A_1	I	Address field LSBs and Address Counter Preset Inputs
A	I	Address Inputs
DQ_A, DQ_B, DQ_C, DQ_D	I/O	Data Input and Output pins
$\overline{BA}$, $\overline{BB}$, $\overline{BC}$, $\overline{BD}$	I	Byte Write Enable for DQ_A, DQ_B, DQ_C, DQ_D I/Os; active low
NC	—	No Connect
CK	I	Clock Input Signal; active high
$\overline{CKE}$	I	Clock Enable; active low
$\overline{W}$	I	Write Enable; active low
$\overline{E1}$, $\overline{E3}$	I	Chip Enable; active low
E2	I	Chip Enable; active high
$\overline{G}$	I	Output Enable; active low
ADV	I	Burst address counter advance enable; active high
LODRV	I	Low Drive strength control (active high) Low = High Drive, High = Low Drive
ZZ	I	Sleep mode control; active high
$\overline{LBO}$	I	Linear Burst Order mode; active low
TMS	I	Scan Test Mode Select
TDI	I	Scan Test Data In
TDO	O	Scan Test Data Out
TCK	I	Scan Test Clock
MCH	—	Must Connect High (165-FBGA only)
V_{DD}	I	Core power supply
V_{SS}	I	I/O and Core Ground
V_{DDQ}	I	Output driver power supply

Functional Details

Clocking

All inputs *except* Output Enable, Linear Burst Order, and Sleep are synchronized to rising clock edges. Deasserting Clock Enable ($\overline{CKE}$ high) blocks the Clock input from reaching the RAM's internal circuits, thus suspending operation. Failure to observe Clock Enable set-up or hold requirements will result in erratic operation.

Read and Write Operations

Single cycle read and write operations are initiated with ADV held low in order to load the new address. The device is activated by asserting all three Chip Enables ($\overline{E1}$, E2, and $\overline{E3}$). Deassertion of any Chip Enable deactivates the device.

Read operation starts when the following conditions occur at a rising clock edge: $\overline{CKE}$ low, all three chip enables ($\overline{E1}$, E2, and $\overline{E3}$) active, write enable ($\overline{W}$) high, and ADV low. The value of address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read is in progress and allows the requested data to propagate to the input of the output register. At the next rising clock edge the read data propagates through the output register and onto the output pins.

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Write operation starts when the RAM is selected, $\overline{CKE}$ is active, and $\overline{W}$ is sampled low at the rising clock edge. The Byte Write Enables ($\overline{BA}$ – $\overline{BB}$ or $\overline{BA}$ – $\overline{BD}$) determine which bytes will be written; all or none may be activated. A write cycle with no active Byte Write Enable is a no-op cycle.

Partial Truth Table (x36)

Function	$\overline{W}$	$\overline{BA}$	$\overline{BB}$	$\overline{BC}$	$\overline{BD}$
Read	H	X	X	X	X
Write Byte "a"	L	L	H	H	H
Write Byte "b"	L	H	L	H	H
Write Byte "c"	L	H	H	L	H
Write Byte "d"	L	H	H	H	L
Write all Bytes	L	L	L	L	L
Write Abort/NOP	L	H	H	H	H

Operation

This device is pipelined, with double late write functionality, matching the write command versus data pipeline length (2 cycles) to the read command versus data pipeline length (2 cycles). At the first rising clock edge, Enable, Write, Byte Write(s), and Address are registered. The Data In associated with that address is required at the third rising clock edge.

Burst Cycles

These devices sustain 100% bus bandwidth by eliminating turnaround cycles, and also by performing multiple back-to-back reads or writes. The on-chip burst address generator further simplifies burst read or write implementations. Driving ADV high commands the device to advance the internal address counter and use the generated address to read or write. The starting address for the first cycle in a burst is loaded into the device by driving ADV low.

Burst Order

The burst sequence is determined by the Linear Burst Order pin ($\overline{LBO}$): Low = Linear, High = Interleaved.

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note:
In both cases, the burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Output Strength

The LODRV pin selects either nominal drive strength (LODRV low) for multi-drop bus applications or low drive strength (LODRV floating or high) for point-to-point applications.

Sleep Mode

Sleep mode is a low current "power-down" mode in which the device is deselected and current is reduced to I_{SB2}. The mode is controlled by ZZ, an asynchronous, active high input. During normal operation, ZZ must be pulled low, either by the user or by its internal pull down resistor. When ZZ is pulled high, the device enters a Sleep mode after 2 cycles; the internal state of the device is preserved. When ZZ returns to low, the device resumes normal operation after 2 cycles of wake up time.

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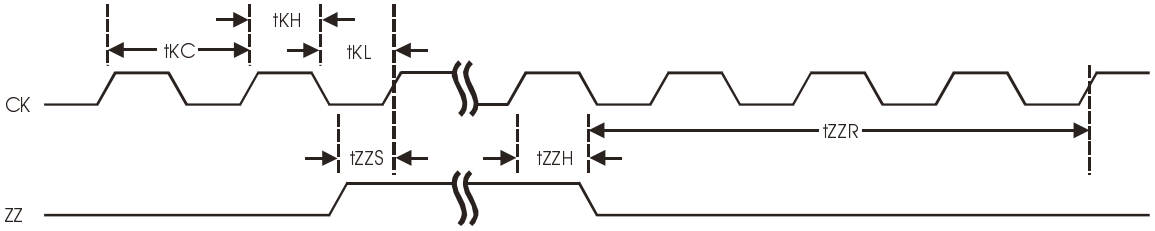
In Sleep mode, all inputs except ZZ are disabled and all outputs go to High-Z. When the ZZ pin is driven high, I_{SB2} is guaranteed after time tZZI. Because ZZ is an asynchronous input, current or pending operations may not be properly completed if ZZ is asserted; Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode, only Deselect or Read commands may be applied during tZZR.



Mode Pin Functions

Mode	Pin	Pulled?	State	Function
Burst Order Control	$\overline{LBO}$	no	L	Linear Burst
			H	Interleaved Burst
Power Down Control	ZZ	Down	L or NC	Active
			H	Standby, $I_{DD} = I_{SB}$
Drive Strength Control	LODRV	Up	L	High Drive
			H or NC	Low Drive

Note: There is a pull-up on the LODRV pin and a pull-down on the ZZ pin; if these pins are unconnected, the device operates in the default states (specified by "NC" in the table).

Synchronous Truth Table

Operation	Type	Address	CK	$\overline{CKE}$	ADV	$\overline{W}$	$\overline{Bx}$	$\overline{E1}$	E2	$\overline{E3}$	$\overline{G}$	ZZ	DQ	Notes
Read Cycle, Begin Burst	R	External	L-H	L	L	H	X	L	H	L	L	L	Q	
Read Cycle, Continue Burst	B	Next	L-H	L	H	X	X	X	X	X	L	L	Q	1,2
Dummy Read, Begin Burst (NOP)	R	External	L-H	L	L	H	X	L	H	L	H	L	High-Z	
Dummy Read, Continue Burst (NOP	B	Next	L-H	L	H	X	X	X	X	X	H	L	High-Z	1,2
Write Cycle, Begin Burst (NOP)	W	External	L-H	L	L	L	L	L	H	L	X	L	D	3
Write Cycle, Continue Burst (NOP)	B	Next	L-H	L	H	X	L	X	X	X	X	L	D	1,2,3
Write Abort, Begin Burst	W	External	L-H	L	L	L	H	L	H	L	x	L	High-Z	
Write Abort, Continue Burst	B	Next	L-H	L	H	X	H	X	X	X	X	L	High-Z	1,2,3
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	H	X	X	X	L	High-Z	
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	X	X	H	X	L	High-Z	
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	X	L	X	X	L	High-Z	
Deselect Cycle	D	None	L-H	L	L	L	H	L	H	L	X	L	High-Z	1
Deselect Cycle, Continue	D	None	L-H	L	H	X	X	X	X	X	X	L	High-Z	1
Sleep Mode		None	X	X	X	X	X	X	X	X	X	H	High-Z	
Clock Edge Ignore, Stall		Current	L-H	H	X	X	X	X	X	X	X	L	-	4

Notes: X = Don't Care; H = Logic High; L = Logic Low; $\overline{Bx}$ "High" = All Byte Writes are high; $\overline{Bx}$ "L" = At least one Byte Write is low. All inputs *except* $\overline{G}$ and ZZ must meet setup and hold times of rising clock edge. Wait states can be inserted by setting $\overline{CKE}$ high. Device circuitry ensures that all outputs are in High Z during power-up. A 2-bit burst counter is incorporated.

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1. All Continue Bursts (read or write) use the same control inputs. A Deselect Continue can only occur after a Deselect.
2. The address counter is incremented for all Burst Continue cycles.
3. $\overline{G}$ can be wired low to minimize the number of control signals provided to the device. Output drivers will automatically turn off during write cycles.
4. If $\overline{CKE}$ High occurs during a read, the DQ bus remains active (Low Z). If $\overline{CKE}$ High occurs during a write, the bus remains in High Z.

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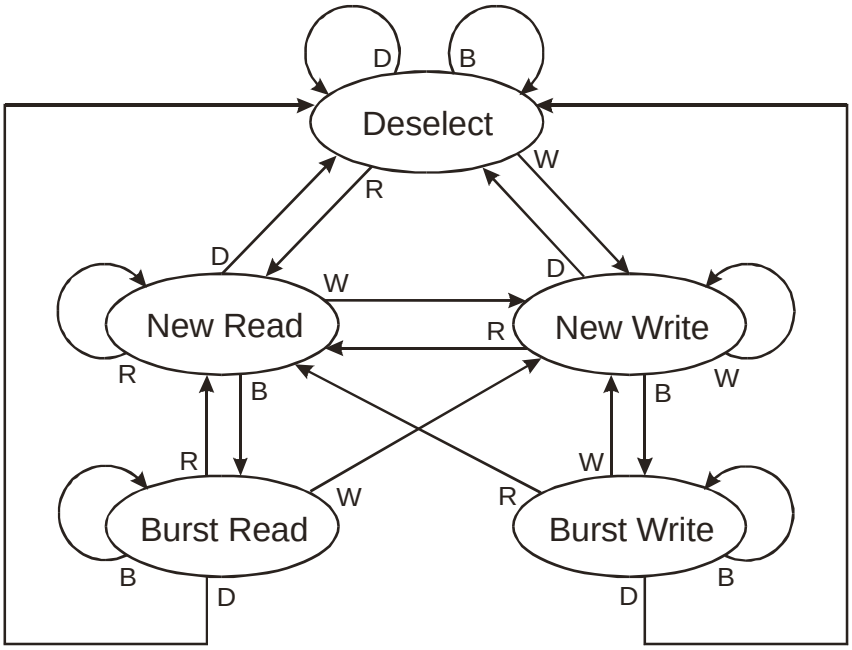
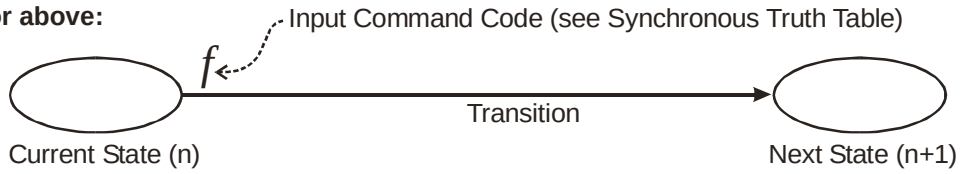
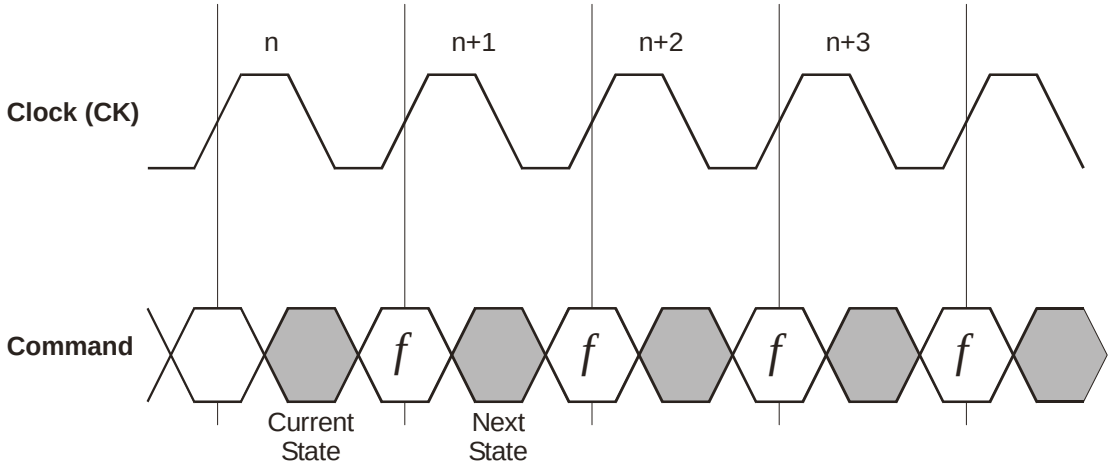
State Diagram: Read/Write Control



Note: The Hold command ($\overline{CKE}$ low) is not shown because it prevents any state change.

Key for above:





Current State and Next State Definition for State Diagram

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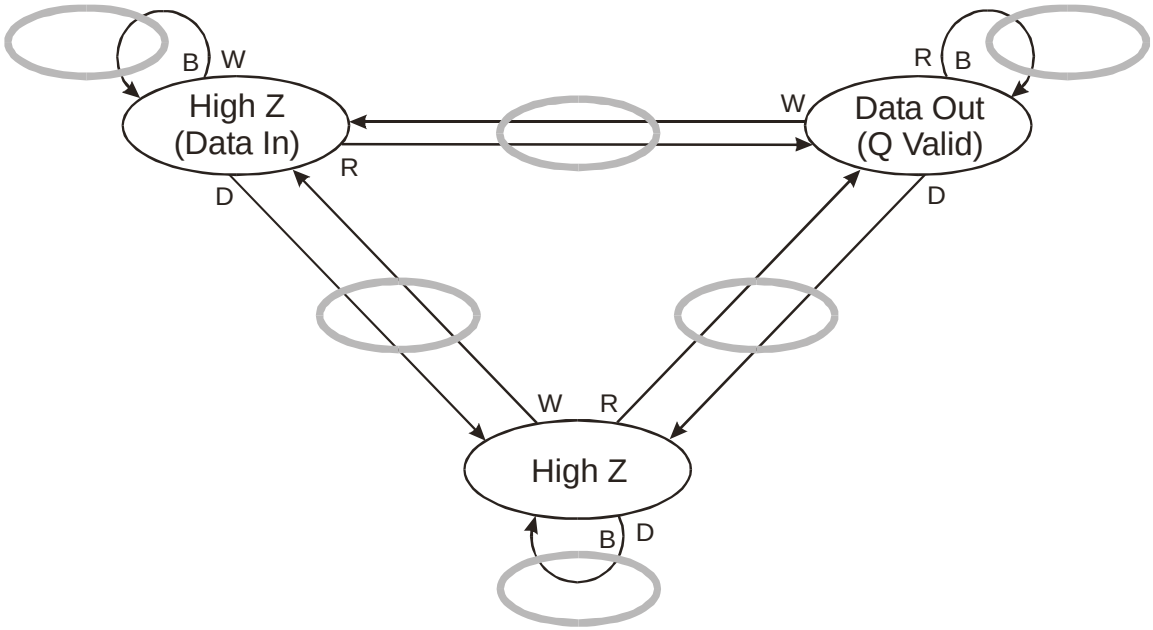
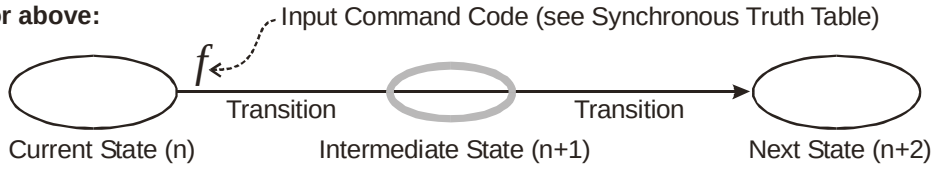
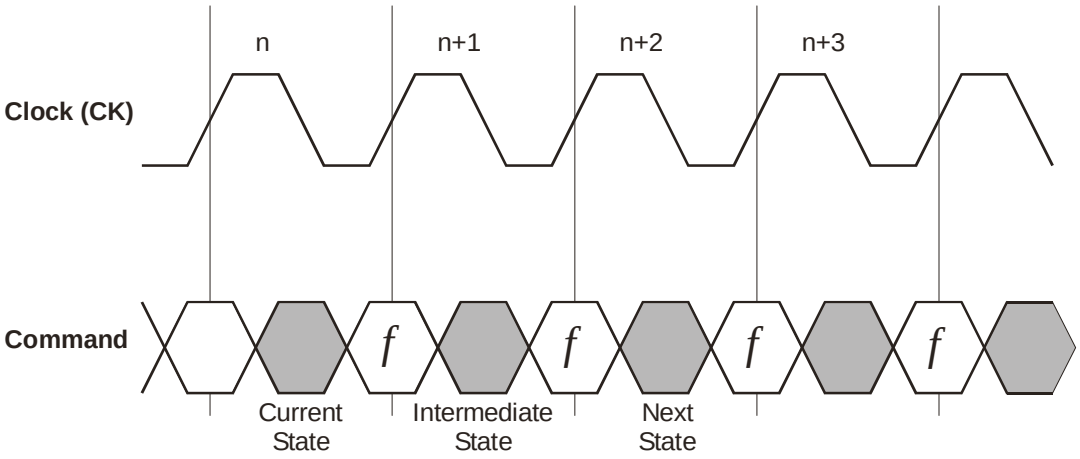
State Diagram: Data I/O



Note: The Hold command ($\overline{CKE}$ low) is not shown because it prevents any state change.

Key for above:





Current State and Next State Definition for State Diagram

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Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 3.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to 3.6	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DDQ} +0.5 (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–55 to 125	°C
T_{BIAS}	Temperature Under Bias	–55 to 125	°C

Note: Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings for an extended period of time may affect reliability of this component.

Voltages

Note: In all cases, input under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

Power Supply Voltage Ranges:

Parameter	Symbol	Min.	Typ.	Max.	Unit
2.5 V Supply Voltage	V_{DD}	2.3	2.5	2.7	V
1.8 V V_{DDQ} I/O Supply Voltage	V_{DDQ1}	1.7	1.8	1.95	V
2.5 V V_{DDQ} I/O Supply Voltage	V_{DDQ2}	2.3	2.5	2.7	V

Range Logic Levels:
(both V_{DDQ1} and V_{DDQ2})

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	0.6*V_{DDQ}	—	V_{DDQ} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.3*V_{DDQ}	V

Recommended Operating Temperatures

Parameter	Symbol	Range	Min.	Typ.	Max.	Unit
Ambient Temperature	T_A	Commercial	0	25	70	°C
		Industrial	–40	25	85	°C
Case Temperature	T_C	Commercial	0	25	100	°C
		Industrial	–40	25	105	°C

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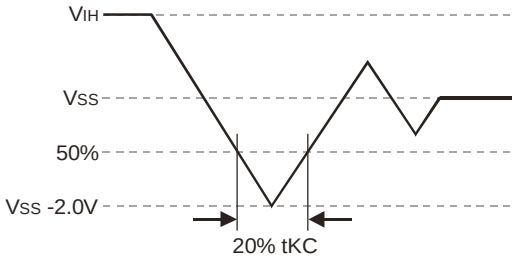
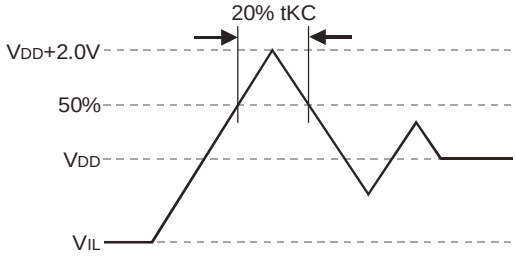
Undershoot Measurement and Timing



Overshoot Measurement and Timing



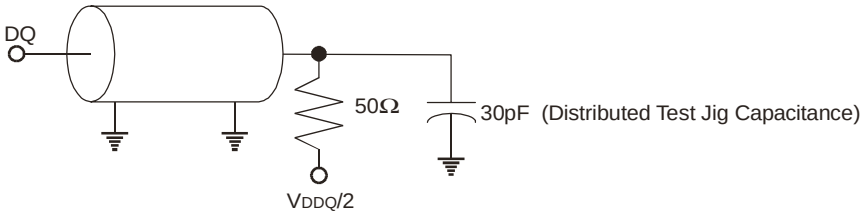
Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 2.5 V)

Parameter (sample tested)	Symbol	Test conditions	Typ.	Max.
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0 V	6	7

AC Test Conditions

Parameter	Conditions	Notes
Input high level	V_{DDQ} – 0.2 V	Include scope and jig capacitance. Test conditions as specified with output loading as shown in the figure below unless otherwise noted. Device is deselected as defined by the Truth Table.
Input low level	0.2 V	
Input slew rate	1 V/ns	
Input reference level	V_{DDQ}/2	
Output reference level	V_{DDQ}/2	
Output load	see figure below	



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DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DDQ}	–1 uA	1 uA
ZZ Input Current	I_{IN1}	$V_{DDQ} \geq V_{IN} \geq V_{IH}$	–1 uA	1 uA
		$0\ V \leq V_{IN} \leq V_{IH}$	–1 uA	100 uA
LODRV Input Current	I_{IN2}	$V_{DDQ} \geq V_{IN} \geq V_{IL}$	–100 uA	1 uA
		$0\ V \leq V_{IN} \leq V_{IL}$	–1 uA	1 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH1}	I_{OH} = –8 mA, V_{DDQ} = 1.775 V	1.4 V	—
Output High Voltage	V_{OH2}	I_{OH} = –8 mA, V_{DDQ} = 2.375 V	1.7 V	—
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	0.4 V

Operating Currents (mA)

Parameter	Test Conditions	Mode	Symbol	-250		-200		-166	
				0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C
Operating Current	Device Selected; All other inputs ≥V_{IH} or ≤ V_{IL} Output open	**(x36)**	I_{DD}	tbd	tbd	tbd	tbd	tbd	tbd
			I_{DDQ}	tbd	tbd	tbd	tbd	tbd	tbd
		(x18)	I_{DD}	tbd	tbd	tbd	tbd	tbd	tbd
			I_{DDQ}	tbd	tbd	tbd	tbd	tbd	tbd
Standby Current	ZZ ≥ V_{DDQ} – 0.2 V	—	I_{SB}	tbd	tbd	tbd	tbd	tbd	tbd
Deselect Current	Device Deselected; All other inputs ≥ V_{IH} or ≤ V_{IL}	—	I_{DD}	tbd	tbd	tbd	tbd	tbd	tbd

Notes: **1.** I_{DD} and I_{DDQ} apply to any combination of V_{DD}, V_{DDQ1}, and V_{DDQ2} operation.
2. All parameters listed are worst case scenario.

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AC Electrical Characteristics (ns)

Parameter	Symbol	-250		-200		-166	
		Min	Max	Min	Max	Min	Max
Clock Cycle Time	tKC	4.0	—	5.0	—	6.0	—
Clock to Output Valid	tKQ	—	2.5	—	3.0	—	3.5
Clock to Output Invalid	tKQX	1.5	—	1.5	—	1.5	—
Clock to Output in Low-Z	tLZ_1	1.5	—	1.5	—	1.5	—
Setup time	tS	1.3	—	1.4	—	1.5	—
Hold Time	tH	0.2	—	0.4	—	0.5	—
Clock HIGH Time	tKH	1.8	—	2.0	—	2.2	—
Clock LOW Time	tKL	1.8	—	2.0	—	2.2	—
Clock to Output in High-Z	tHZ_1	1.5	2.5	1.5	3.0	1.5	3.0
$\overline{G}$ to Output Valid	tOE	—	2.5	—	3.2	—	3.5
$\overline{G}$ to output in Low-Z	$tOLZ_1$	0	—	0	—	0	—
$\overline{G}$ to output in High-Z	$tOHZ_1$	–	2.5	—	3.0	—	3.0
ZZ setup time	$tZZS_2$	5	—	5	—	5	—
ZZ hold time	$tZZH_2$	1	—	1	—	1	—
ZZ recovery	tZZR	20	—	20	—	20	—

Notes:

1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

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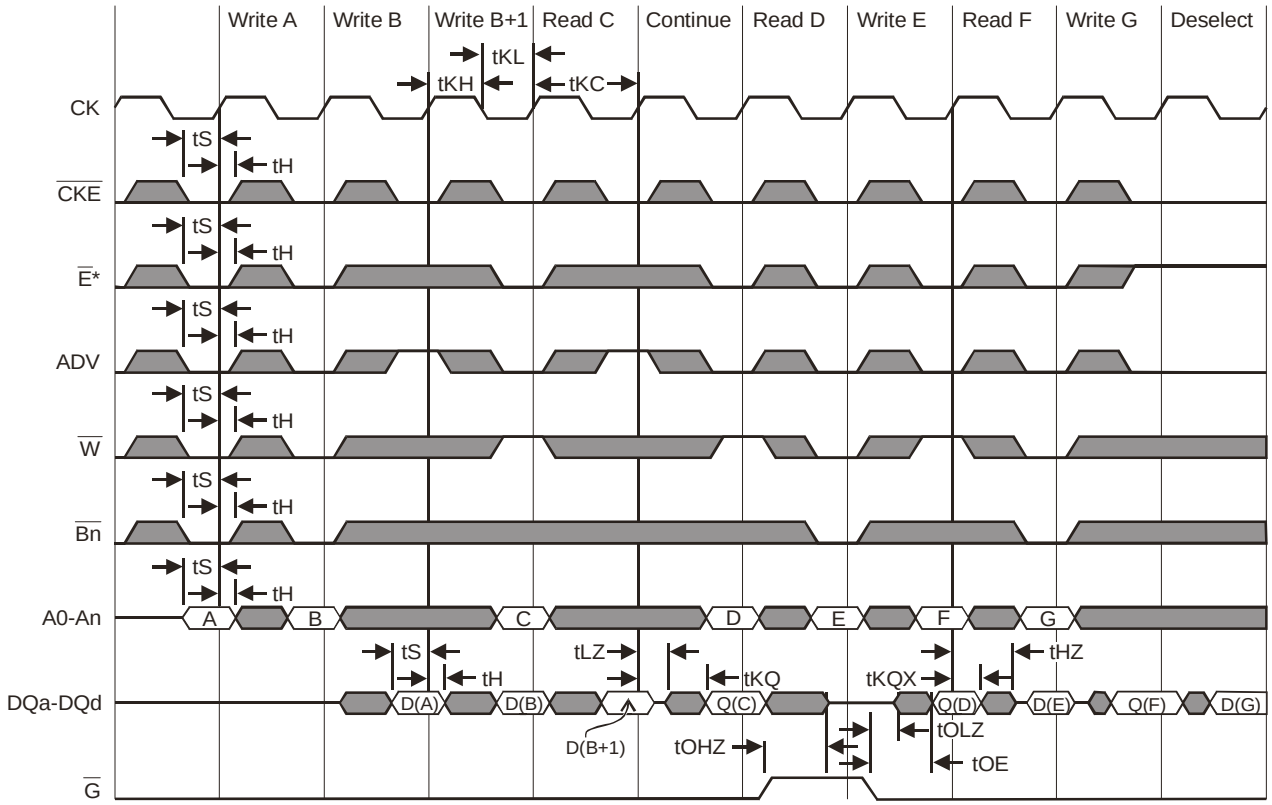
NBT Timing



*$\overline{E}$ = High (False) if $\overline{E1}$ = 1 or E2 = 0 or $\overline{E3}$ = 1

JTAG Port Operation

Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with V_{DD}. The JTAG output drivers are powered by V_{DDQ}.

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits. To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either V_{DD} or V_{SS}. TDO should be left unconnected.

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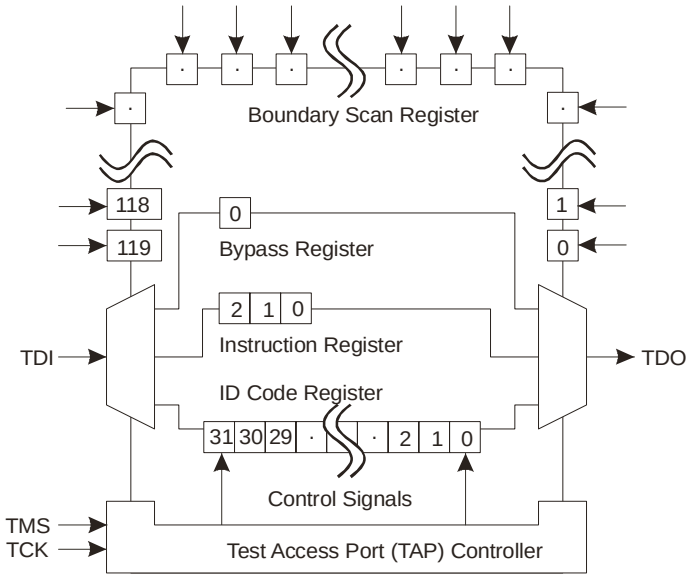
JTAG TAP Block Diagram



JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note: This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automatically at power-up.

JTAG Port Registers

The various JTAG registers, referred to as Test Access Port or TAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

Bypass Register

The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

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Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAM's I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Contents

	Die Revision Code				Not Used												I/O Configuration				Tezzaron Semiconductor JEDEC Vendor ID Code											Presence Register
Bit#	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
x36	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1
x18	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	1	0	1	1	0	0	1

JTAG Tap Controller Instruction Set

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state.

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Instruction Summary

Note: Instruction codes expressed in binary, MSB on left, LSB on right.

Instruction	Code	Description
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.
IDCODE	001	Preloads ID Register and places it between TDI and TDO. **Default instruction** – automatically loaded at power-up and in test-logic-reset state.
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.
RFU	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.
TEZZARON	101	Tezzaron private instruction.
RFU	110	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.
BYPASS	111	Places Bypass Register between TDI and TDO.

Instruction Descriptions

BYPASS

BYPASS causes the Bypass Register to be placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state; it allows the board level scan path to be shortened to facilitate testing of other devices in the path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When SAMPLE / PRELOAD is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAM's input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with any input or I/O pin. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAP's input data capture set-up plus hold time (tTS plus tTH). The RAM's clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data using SAMPLE/PRELOAD, and then EXTEST is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using EXTEST. When EXTEST is selected, the state of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK. In the Capture-DR state, the RAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

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IDCODE

IDCODE causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

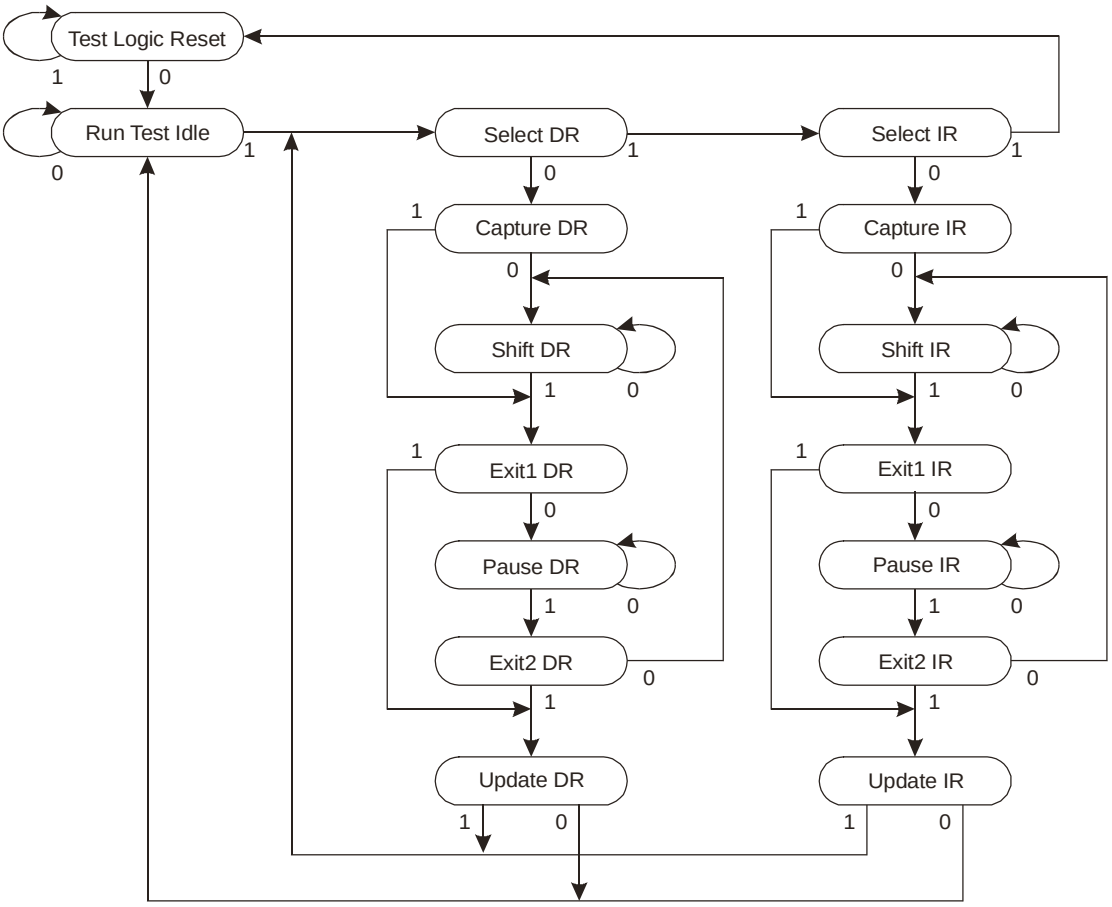
SAMPLE-Z

If SAMPLE-Z is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

RFU

These instructions are Reserved for Future Use. In this device they replicate the BYPASS instruction.

JTAG Tap Controller State Diagram



JTAG Port AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	tTKC	50	—	ns
TCK Low to TDO Valid	tTKQ	—	20	ns
TCK High Pulse Width	tTKH	20	—	ns
TCK Low Pulse Width	tTKL	20	—	ns
TDI & TMS Set Up Time	tTS	10	—	ns
TDI & TMS Hold Time	tTH	10	—	ns

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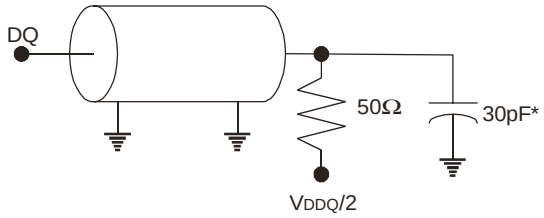
JTAG Port AC Test Conditions

Parameter	Conditions
Input high level	VDDQ – 0.2 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	VDDQ/2
Output reference level	VDDQ/2

Notes: Include scope and jig capacitance.
Test conditions as shown unless otherwise noted.

JTAG Port AC Test Load



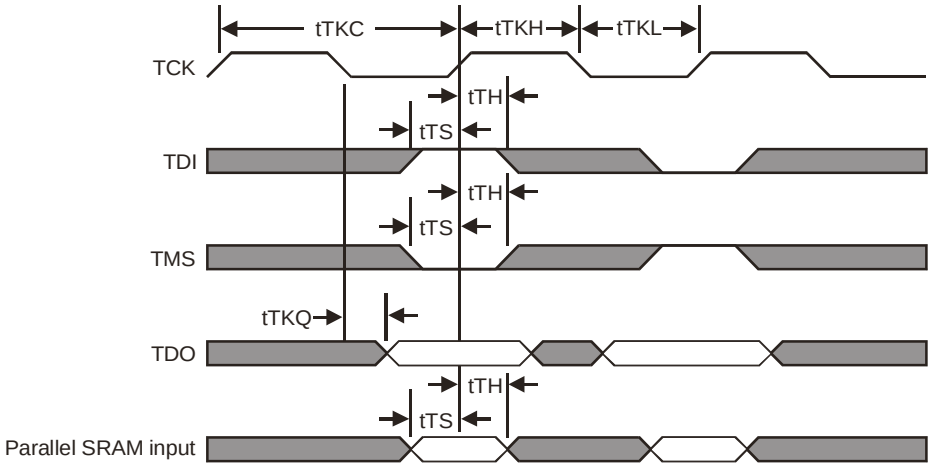
*Distributed Test Jig Capacitance

JTAG Port Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
1.8 V Test Port Input High Voltage	VIHJ1	0.6 * VDDQ1	VDDQ1 +0.3	V	Input under/overshoot voltage must be –2 V > Vi < VDDQn +2 V, not to exceed 3.6 V maximum, with a pulse width not to exceed 20% tTKC.
1.8 V Test Port Input Low Voltage	VILJ1	–0.3	0.3 * VDDQ1	V	
2.5 V Test Port Input High Voltage	VIHJ2	0.6 * VDDQ2	VDDQ2 +0.3	V	
2.5 V Test Port Input Low Voltage	VILJ2	–0.3	0.3 * VDDQ2	V	
TMS, TCK and TDI Input Leakage Current (high)	IINHJ	–300	1	uA	VILJn ≤ VIN ≤ VDDn
TMS, TCK and TDI Input Leakage Current (low)	IINLJ	–1	100	uA	0 V ≤ VIN ≤ VILJn
TDO Output Leakage Current	IOLJ	–1	1	uA	Output Disable, VOUT = 0 to VDDn
Test Port Output High Voltage	VOHJ	VDDQ – 0.4 V	—	V	IOHJ = –4 mA
Test Port Output Low Voltage	VOLJ	—	0.4	V	IOLJ = + 4 mA
Test Port Output CMOS High	VOHJC	VDDQ – 100 mV	—	V	IOHJC = –100 uA
Test Port Output CMOS Low	VOLJC	—	100 mV	V	IOLJC = +100 uA

Note: The TDO output driver is served by the VDDQ supply.

JTAG Port Timing Diagram



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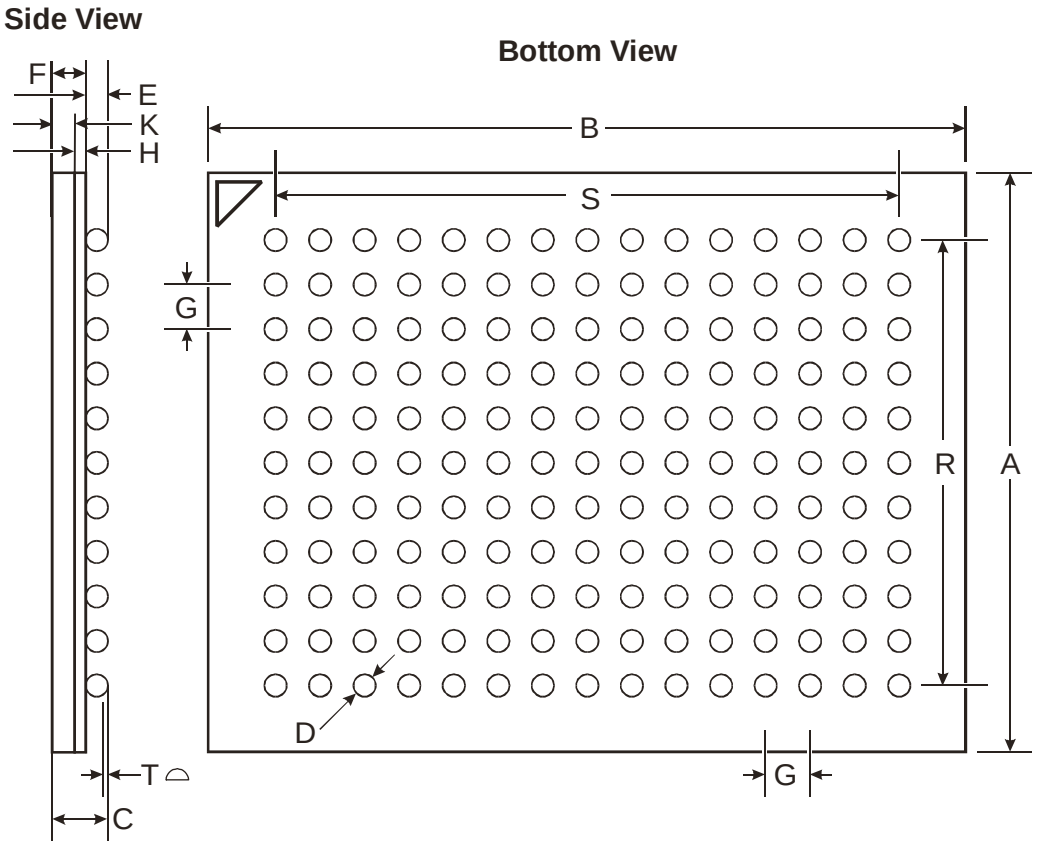
165-FBGA Package Drawing

11 x 15 Array – 15 x 17 x 1.40 mm – 1.0 mm Pitch



165-FBGA Package Dimensions

Symbol	Description	Min	Nom	Max	Symbol	Description	Min	Nom	Max
A	Width	14.90	15	15.10	G	Width between Balls	—	1.00	—
B	Length	16.90	17	17.10	H	Board Thickness	—	0.36	—
C	Package Height (including ball)	—	—	1.40	K	Package Height above board	0.48	0.53	0.58
D	Ball Diameter	0.40	0.45	0.50	R	Width of package between balls	—	10.00	—
E	Ball Height	0.25	0.35	0.40	S	Length of package between balls	—	14.00	—
F	Package Height (excluding ball)	0.79	0.89	1.00	T	Variance of Ball Height	—	0.15	—

All units: mm **All units: mm**

165-FBGA Thermal Characteristics

Package	Junction to Ambient (θ) (°C/W)			Junction to Case (θ) (°C/W)
	0 m/s	1 m/s	2 m/s	
165-FBGA	15.1	13.2	11.9	2.0

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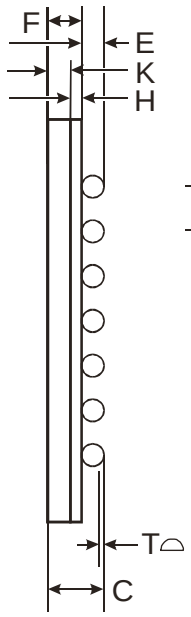
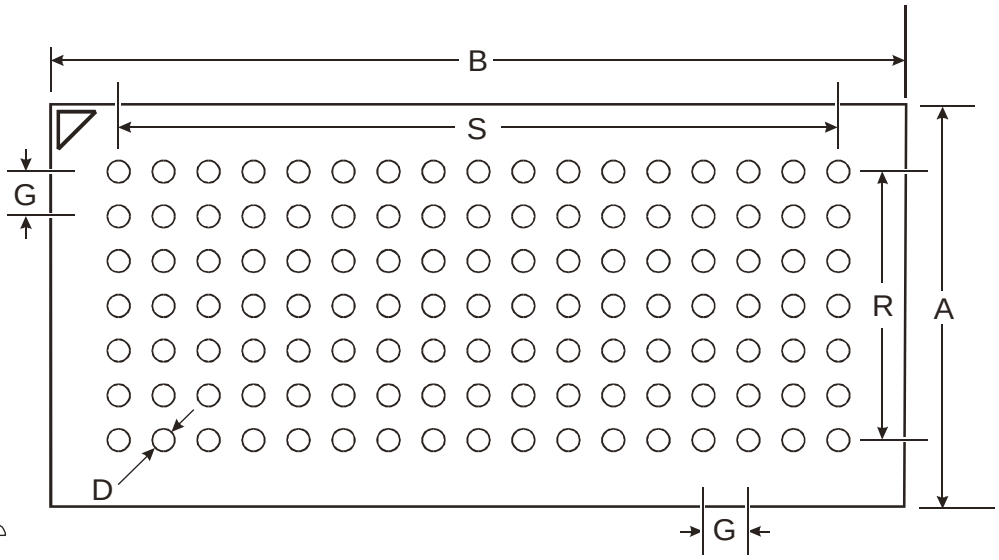
119-FBGA Package Drawing

7 x 17 Array – 14 x 22 x 1.99 mm – 1.27 mm Pitch

Side View



Bottom View



119-FBGA Package Dimensions

Symbol	Description	Min	Nom	Max	Symbol	Description	Min	Nom	Max
A	Width	13.9	14.0	14.1	G	Width between Balls	—	1.27	—
B	Length	21.9	22.0	22.1	H	Board Thickness	0.51	0.56	0.61
C	Package Height (including ball)	1.73	1.86	1.99	K	Package Height above board	0.65	0.70	0.75
D	Ball Diameter	0.60	0.75	0.90	R	Width of package between balls	—	7.62	—
E	Ball Height	0.50	0.60	0.70	S	Length of package between balls	—	20.32	—
F	Package Height (excluding ball)	—	—	1.36	T	Variance of Ball Height	—	0.15	—

All units: mm **All units: mm**

119-FBGA Thermal Characteristics

Package	Junction to Ambient (θ) (°C/W)			Junction to Case (θ) (°C/W)
	0 m/s	1 m/s	2 m/s	
119-FBGA	17.7	16.0	14.1	2.8

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Document History

Datasheet for TSC2L72T18 / 36

Revision Number	Date	Changes
1.0 – 1.3	various	Pre-release data
1.4	November 14, 2005	Changed speed grades, reworked package dimensions.
1.5	23 January 2007	Removed x72 configuration, removed 209 FBGA package, corrected typos.

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