

**72Mb Synchronous Double Transfer Rate (DTRII™) 3T-iRAM™
With Separate I/O**

**Burst of 2
SRAM-Compatible**

Features

- Error-resistant 3T-iRAM™ technology
- DTRII™ Interface with Separate I/O buses
- Fully pin-compatible with DDRII and SigmaSIO-II™ SRAMs
- JEDEC-standard pinout and package
- Burst of 2 Read and Write (Byte Writes)
- 1.8 V +100/-100 mV core power supply
- 1.5 V or 1.8 V HSTL Interface
- Synchronous internally self-timed Writes
- Fully coherent read and write pipelines
- ZQ pin for programmable output drive strength
- IEEE 1149.1 JTAG-compliant Boundary Scan
- 165-bump 15mm x 17mm BGA, 1 mm bump pitch
- Pin-compatible with 9Mb, 18Mb, 36Mb, and 144Mb devices

Options

- Configurations: 8M x 9 S09
4M x 18 S18
2M x 36 S36
- Package: 165 FBGA B
- Speed (MHz): 333 MHz -333
300 MHz -300
267 MHz -267
200 MHz -200
167 MHz -167

Marking

Part number example: **TSC3D272S18B-300**

Functional Description

3T-iRAM™ is a unique type of dynamic memory. Tezzaron has crafted these pseudo-static devices to provide entirely SRAM-compatible interfaces and timing. The unique design of these 3T memories provides soft error rates up to 10 times lower than equivalent high-speed, high-density SRAMs.

DTRII™ is a double transfer rate interface that is implemented with Separate I/O architecture in these devices, making them drop-in compatible with DDRII and SigmaSIO-II™ SRAMs.

These synchronous 72Mb 3T-iRAM devices employ two input register clocks, K and \bar{K} . The user can manipulate the output register clocks quasi-independently with C and \bar{C} . These clocks are four independent single-ended clock inputs, not differential inputs. If the C clocks are tied high, the K clocks are routed internally to fire the output registers instead.

These devices always transfer data in two packets. A0 is internally set to 0 for the first transfer of a data burst and automatically incremented to 1 for the second transfer.

Speed Parameter Synopsis:
(all units ns)

	-333	-300	-267	-250	-200	-167
tKHKH	3.00	3.30	3.75	4.00	5.00	6.00
tKHQV	0.45	0.45	0.45	0.45	0.45	0.50

Pin Configurations

2M x 36: Top View

	1	2	3	4	5	6	7	8	9	10	11	
A	\overline{CQ}	Vss/288M	SA	R/ \overline{W}	$\overline{BW2}$	\overline{K}	$\overline{BW1}$	\overline{LD}	SA	Vss/144M	CQ	A
B	Q27	Q18	D18	SA	$\overline{BW3}$	K	$\overline{BW0}$	SA	D17	Q17	Q8	B
C	D27	Q28	D19	Vss	SA	SA	SA	Vss	D16	Q7	D8	C
D	D28	D20	Q19	Vss	Vss	Vss	Vss	Vss	Q16	D15	D7	D
E	Q29	D29	Q20	VDDQ	Vss	Vss	Vss	VDDQ	Q15	D6	Q6	E
F	Q30	Q21	D21	VDDQ	VDD	Vss	VDD	VDDQ	D14	Q14	Q5	F
G	D30	D22	Q22	VDDQ	VDD	Vss	VDD	VDDQ	Q13	D13	D5	G
H	\overline{Doff}	VREF	VDDQ	VDDQ	VDD	Vss	VDD	VDDQ	VDDQ	VREF	ZQ	H
J	D31	Q31	D23	VDDQ	VDD	Vss	VDD	VDDQ	D12	Q4	D4	J
K	Q32	D32	Q23	VDDQ	VDD	Vss	VDD	VDDQ	Q12	D3	Q3	K
L	Q33	Q24	D24	VDDQ	Vss	Vss	Vss	VDDQ	D11	Q11	Q2	L
M	D33	Q34	D25	Vss	Vss	Vss	Vss	Vss	D10	Q1	D2	M
N	D34	D26	Q25	Vss	SA	SA	SA	Vss	Q10	D9	D1	N
P	Q35	D35	Q26	SA	SA	C	SA	SA	Q9	D0	Q0	P
R	TDO	TCK	SA	SA	SA	\overline{C}	SA	SA	SA	TMS	TDI	R

Notes: $\overline{BW0}$ controls writes to DQ0:DQ8;
 $\overline{BW1}$ controls writes to DQ9:DQ17;
 $\overline{BW2}$ controls writes to DQ18:DQ26;
 $\overline{BW3}$ controls writes to DQ27:DQ35.

4M x 18: Top View

	1	2	3	4	5	6	7	8	9	10	11	
A	\overline{CQ}	Vss/144M	SA	R/ \overline{W}	$\overline{BW1}$	\overline{K}	NC	\overline{LD}	SA	SA	CQ	A
B	NC	Q9	D9	SA	NC	K	$\overline{BW0}$	SA	NC	NC	Q8	B
C	NC	NC	D10	Vss	SA	SA	SA	Vss	NC	Q7	D8	C
D	NC	D11	Q10	Vss	Vss	Vss	Vss	Vss	NC	NC	D7	D
E	NC	NC	Q11	VDDQ	Vss	Vss	Vss	VDDQ	NC	D6	Q6	E
F	NC	Q12	D12	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	Q5	F
G	NC	D13	Q13	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	D5	G
H	\overline{Doff}	VREF	VDDQ	VDDQ	VDD	Vss	VDD	VDDQ	VDDQ	VREF	ZQ	H
J	NC	NC	D14	VDDQ	VDD	Vss	VDD	VDDQ	NC	Q4	D4	J
K	NC	NC	Q14	VDDQ	VDD	Vss	VDD	VDDQ	NC	D3	Q3	K
L	NC	Q15	D15	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	Q2	L
M	NC	NC	D16	Vss	Vss	Vss	Vss	Vss	NC	Q1	D2	M
N	NC	D17	Q16	Vss	SA	SA	SA	Vss	NC	NC	D1	N
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0	P
R	TDO	TCK	SA	SA	SA	\overline{C}	SA	SA	SA	TMS	TDI	R

Notes: $\overline{BW0}$ controls writes to DQ0:DQ8; $\overline{BW1}$ controls writes to DQ9:DQ17

8M x 9: Top View

	1	2	3	4	5	6	7	8	9	10	11	
A	$\overline{\text{CQ}}$	SA	SA	R/ $\overline{\text{W}}$	NC	$\overline{\text{K}}$	NC/144M	$\overline{\text{LD}}$	SA	SA	CQ	A
B	NC	NC	NC	SA	NC	K	$\overline{\text{BW0}}$	SA	NC	NC	Q4	B
C	NC	NC	NC	Vss	SA	SA	SA	Vss	NC	NC	D4	C
D	NC	D5	NC	Vss	Vss	Vss	Vss	Vss	NC	NC	NC	D
E	NC	NC	Q5	VDDQ	Vss	Vss	Vss	VDDQ	NC	D3	Q3	E
F	NC	NC	NC	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	NC	F
G	NC	D6	Q6	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	NC	G
H	$\overline{\text{Doff}}$	VREF	VDDQ	VDDQ	VDD	Vss	VDD	VDDQ	VDDQ	VREF	ZQ	H
J	NC	NC	NC	VDDQ	VDD	Vss	VDD	VDDQ	NC	Q2	D2	J
K	NC	NC	NC	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	NC	K
L	NC	Q7	D7	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	Q1	L
M	NC	NC	NC	Vss	Vss	Vss	Vss	Vss	NC	NC	D1	M
N	NC	D8	NC	Vss	SA	SA	SA	Vss	NC	NC	NC	N
P	NC	NC	Q8	SA	SA	C	SA	SA	NC	D0	Q0	P
R	TDO	TCK	SA	SA	SA	$\overline{\text{C}}$	SA	SA	SA	TMS	TDI	R

Pin Descriptions

Symbol	Type	Description
SA	INPUT	Synchronous address inputs
$\overline{\text{LD}}$	INPUT	Synchronous load; low initiates an access
NC	---	No connect; not connected to die or any other pin
$\overline{\text{R}}/\overline{\text{W}}$	INPUT	Read/Write port select
BW0 – BW3	INPUT	Byte write controls
K / $\overline{\text{K}}$	INPUT	Input clocks (positive/negative)
C / $\overline{\text{C}}$	INPUT	Output clocks (positive/negative)
TMS	INPUT	Test mode select
TDI	INPUT	Test data input
TCK	INPUT	Test clock
TDO	OUTPUT	Test data output
VREF	INPUT	HSTL input reference voltage
ZQ	INPUT	Output impedance matching input
DX	INPUT	Data signals for Write
QX	OUTPUT	Data signals for Read
$\overline{\text{Doff}}$	INPUT	Disable DLL (when low)
CQ / $\overline{\text{CQ}}$	OUTPUT	Output echo clock (positive/negative)
VDD	SUPPLY	Power supply to core; 1.8 V nominal
VDDO	SUPPLY	Isolated output buffer supply; 1.5 V nominal
VSS	SUPPLY	Ground

Functional Details

Clocks

K and $\overline{\text{K}}$ are the input clocks. The rising edges are used to capture all synchronous inputs and, in single-clock mode, to drive out data. All accesses are driven on the rising edge of K.

C and $\overline{\text{C}}$ are the optional output clocks. They can be used to deskew the flight times of various devices back to the controller by delaying data output as much as a few nanoseconds beyond the next rising edges of the K and $\overline{\text{K}}$ clocks. If C and $\overline{\text{C}}$ are tied high at power-on, the device operates in single-clock mode and the K clocks drive the outputs.

CQ and $\overline{\text{CQ}}$ are echo clocks that can be used to simplify data capture in high-speed systems. These clocks are normally referenced with respect to the C clocks; in single-clock mode, they are referenced with respect to the K clocks.

Burst Operations

Read and write operations are synchronous pipelined "burst" operations. In every case where a read or write command is accepted by the RAM, it responds by issuing or accepting two beats of data in one clock cycle, executing data transfers on subsequent rising clock edges, as illustrated in the timing diagrams. It is not possible to stop a burst once it starts; two beats of data are always transferred.

Read and Write Ports

Data flows into the RAM through a dedicated Read port and out through a dedicated Write port. Each port has its own set of dedicated registers. An access (either Read or Write) is initiated on a rising edge of K along with the address for the access. One new access, either Read or Write, may be initiated in every clock cycle without inserting any NOP cycles. Read and Write access cannot be initiated in the same cycle, but operations may overlap.

Read Cycles

A Read access is initiated by asserting R/\overline{W} high and \overline{LD} low on a rising edge of K and presenting the address to the SA pins at the same time. The address is stored in the Read address register. After the next rising edge of K, the RAM produces data out on the Q pins in response to the next rising edge of \overline{C} (or the next rising edge of \overline{K} , if C and \overline{C} are tied high). The second beat of data is transferred in response to the next rising edge of C, for a total of two transfers per address load. Read accesses may be initiated on every rising edge of K to produce a constant stream of output data timed by the rising edges of C and \overline{C} (or K and \overline{K} in single-clock mode).

If all pending Read transactions are completed, internal circuitry tri-states the Q pins after the next rising edge of C.

Write Cycles

A Write access is initiated by asserting both \overline{LD} and R/\overline{W} low on a rising edge of K and presenting the address on the SA pins at the same time. The address is stored in the Write address register. Data in is due at the device inputs on the next rising edge of K and on the subsequent rising edge of \overline{K} , for a total of two transfers per address load. Write accesses may be initiated on every rising edge of K to produce a constant stream of output data timed by the rising edges of K and \overline{K} .

Power-Up Sequence

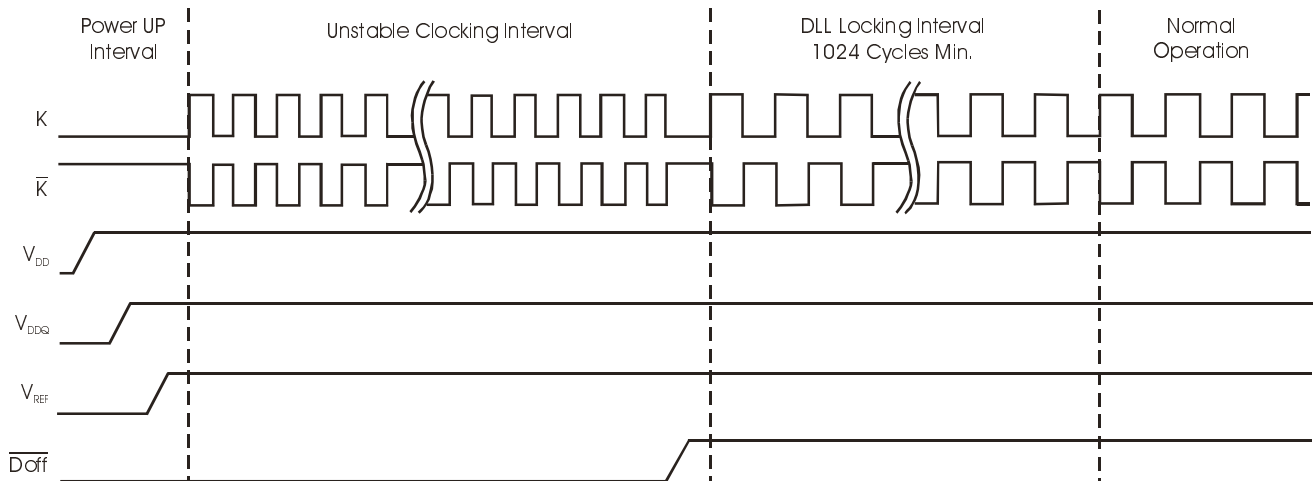
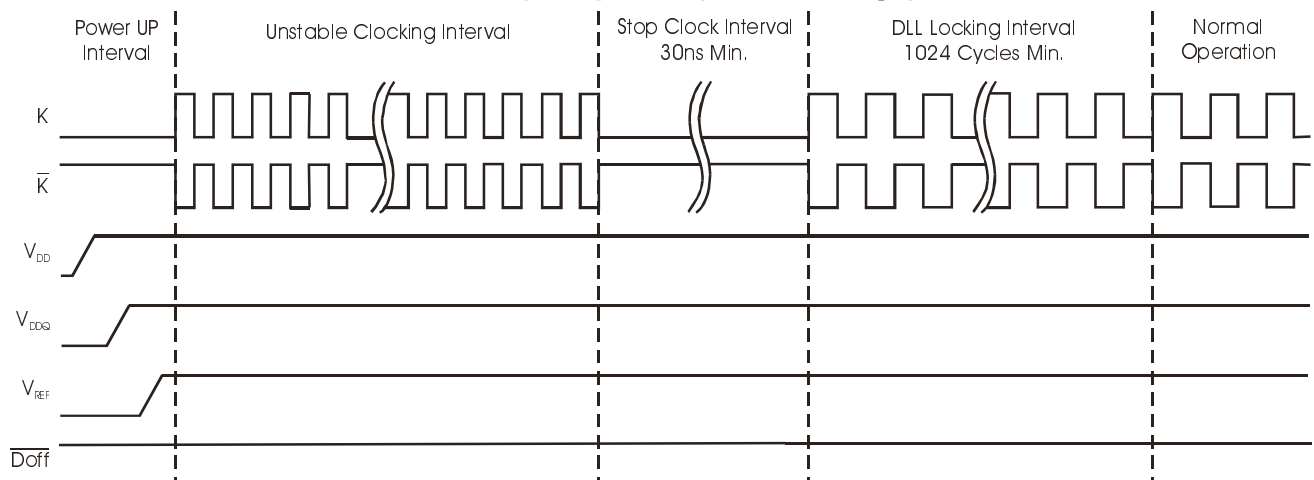
These devices must be powered-up in a specific sequence in order to avoid undefined operations.

1. Power-up and maintain \overline{Doff} at low state.
 - 1a. Apply VDD.
 - 1b. Apply VDDQ.
 - 1c. Apply VREF (may also be applied at the same time as VDDQ).
2. After power is achieved and clocks (K, \overline{K} , C, \overline{C}) are stabilized, change \overline{Doff} to high.
3. An additional 1024 clock cycles are required to lock the DLL after it has been enabled.

Note: If you want to tie \overline{Doff} high with an unstable clock, you must stop the clock for a minimum of 30 ns to reset the DLL after the clocks become stabilized.

DLL Constraints

- The DLL synchronizes to either K or C clock. These clocks should have low phase jitter (see t_{KCVar} on page 13).
- The DLL cannot operate at a frequency lower than 119 MHz.
- If the incoming clock is not stabilized when DLL is enabled, the DLL may lock on the wrong frequency and cause undefined errors or failures during the initial stage.
- If the frequency is changed, DLL reset is required. After reset, a minimum of 1024 cycles is required for DLL lock.

Power-Up Sequence ($\overline{\text{Doff}}$ Controlled)

Power-Up Sequence ($\overline{\text{Doff}}$ Tied High)

Byte Write Control

Byte Write Enable pins are sampled at the same time that D pins are sampled. A high on the Byte Write Enable pin associated with a particular byte (e.g., $\overline{\text{BW0}}$ controls D0–D8 inputs) inhibits the storage of that particular byte, leaving the data at that byte location undisturbed. Any or all of the Byte Write Enable pins may be driven high or low during the data in sample times in a write sequence.

Each write enable command and write address loaded into the RAM provides the base address for a two beat data transfer. The x18 version of the RAM, for example, may write 36 bits in association with each address loaded. Any 9-bit byte may be masked in any write sequence.

Example: x18 Write Sequence Using Byte Write Enables

Data In Sample Time	$\overline{\text{BW0}}$	$\overline{\text{BW1}}$	D0–D8	D9–D17
Beat 1	0	1	Data In	X
Beat 2	1	0	X	Data In

Resulting Write Operation:

Byte 1 D0–D8	Byte 2 D9–D17	Byte 3 D0–D8	Byte 4 D9–D17
Written	Unchanged	Unchanged	Written
Beat 1		Beat 2	

Notes: 1 = input high; 0 = input low; X = input “don’t care”.

Output Register Control

These devices offer two mechanisms for controlling the output data registers. Typically, control is handled by the C and \overline{C} clocks, which can be used to make small phase adjustments in the firing of the output registers by allowing the user to delay driving data out as much as a few nanoseconds beyond the next rising edges of K and \overline{K} . If C and \overline{C} are tied high, the RAM uses K and \overline{K} to control the outputs.

Output Driver Impedance Control

These devices are supplied with optional programmable impedance output drivers that can periodically readjust the impedance to compensate for drifts in supply voltage and temperature.

To enable this feature, the ZQ pin must be connected to VSS via an external resistor, RQ, with a value 5X the value of the intended RAM output impedance. The allowable range of RQ is between 175Ω and 350Ω. An internal calibration sequence occurs every 1024 cycles, and an update is performed during the next available deselected memory cycle. Each update may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps.

To disable this feature, the ZQ pin may be tied directly to VDDQ. The device then runs with a constant minimum impedance; no calibration or adjustments are performed.

Truth Tables

I/O Truth Table

Function	K_n	\overline{LD}	R / \overline{W}	D/Q
Deselect (NOP)	•	1	X	Q = High-Z, D = X
Write	•	0	0	D(A) at $K_{(n+1)}$ • D(A+1) at $\overline{K}_{(n+1)}$ •
Read	•	0	1	Q(A) at $\overline{C}_{(n+1)}$ • Q(A+1) at $C_{(n+2)}$ •
Standby (clock stopped)	stopped	X	X	Previous state

Notes: 1 = High, 0 = Low, X = Don't Care, ↑ = rising edge, A = latched address.

Q is controlled by K clocks if C clocks are not used.

During Standby, it is recommended that $K = \overline{K}$ and $C = \overline{C} = \text{High}$; this enables rapid restart.

Byte Write Enable Truth Table, x18

$\overline{BW0}$	$\overline{BW1}$	D0 – D8	D9 – D17
1	1	X	X
0	1	Data	X
1	0	X	Data
0	0	Data	Data

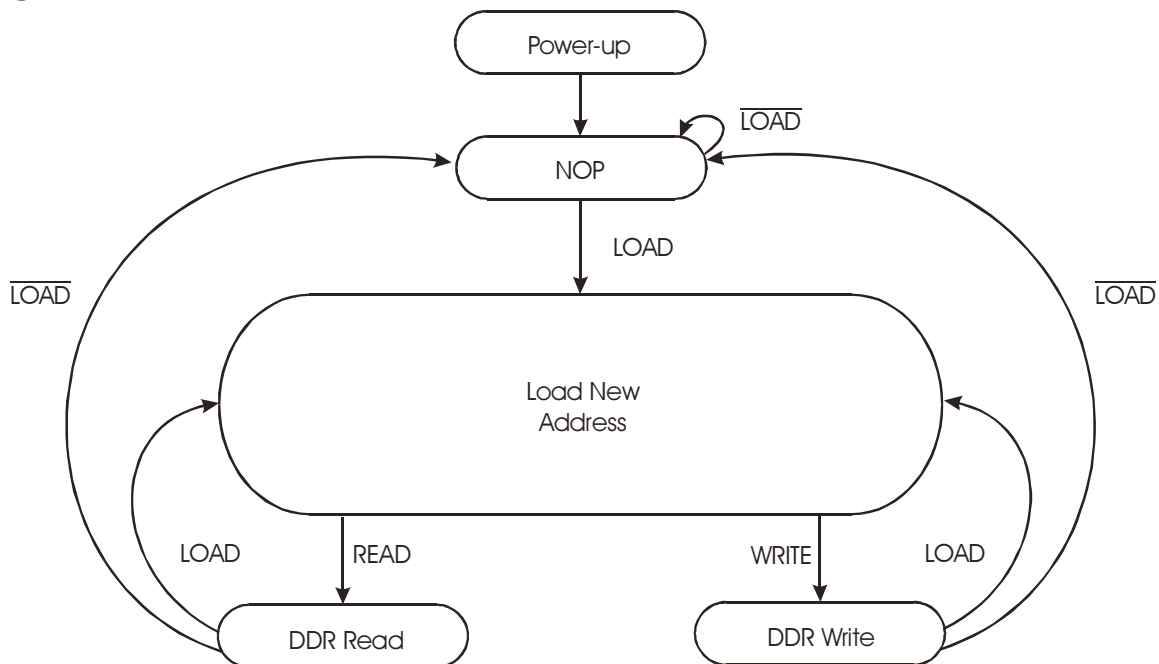
Notes: 1 = High, 0 = Low, X = "Don't Care", Data = valid data to be written to device.

Byte Write Enable Truth Table, x36

BW0	BW1	BW2	BW3	D0 – D8	D9 – D17	D18 – D26	D27 – D35
1	1	1	1	X	X	X	X
0	1	1	1	Data	X	X	X
1	0	1	1	X	Data	X	X
0	0	1	1	Data	Data	X	X
1	1	0	1	X	X	Data	X
0	1	0	1	Data	X	Data	X
1	0	0	1	X	Data	Data	X
0	0	0	1	Data	Data	Data	X
1	1	1	0	X	X	X	Data
0	1	1	0	Data	X	X	Data
1	0	1	0	X	Data	X	Data
0	0	1	0	Data	Data	X	Data
1	1	0	0	X	X	Data	Data
0	1	0	0	Data	X	Data	Data
1	0	0	0	X	Data	Data	Data
0	0	0	0	Data	Data	Data	Data

Notes: 1 = High, 0 = Low, X = “Don’t Care”, Data = valid data to be written to device.

State Diagram



Notes: Uses an internal 1-bit address burst toggle – i.e., first address is A, next internal burst address is A+1.
 “READ” = R/W High; “WRITE” = R/W Low
 “LOAD” = LD Low (load address); “LOAD” = LD High (don’t load address)

Electrical Characteristics

Absolute Maximum Ratings

(All voltages reference to Vss)

Symbol	Description	Value	Unit
VDD	Voltage: VDD pins	-0.5 to 2.9	V
VDDQ	Voltage: VDDQ pins	-0.5 to VDD	V
VREF	Voltage: VREF pins	-0.5 to VDDQ	V
VI/O	Voltage: I/O pins	-0.5 to VDDQ+0.3 (• 2.9 max.)	V
VIN	Voltage: other input pins	-0.5 to VDDQ+0.3 (• 2.9 max.)	V
	Static discharge voltage	>2001	V
IIN	Current: input on any pin	+/- 100	mA dc
IOUT	Current: output on any I/O pin	+/- 100	mA dc
	Latch-up current	>200	mA dc
TJ	Temperature: maximum junction	125	°C
TSTG	Temperature: storage	-55 to 125	°C
TA	Temperature: ambient (power applied)	-10 to 85	°C

Note: Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Extended exposure to conditions exceeding the Recommended Operating Conditions may affect reliability of this component.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	1.70	1.8	1.90	V
I/O Supply Voltage	VDDQ	1.40	1.5	VDD	V
Reference Voltage	VREF	0.68 *	0.75	0.95 *	V
Ambient Temperature (Commercial)	TA	0	25	70	°C
Ambient Temperature (Industrial)	TA	-40	25	85	°C

Notes: Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both $1.4\text{ V} \leq VDDQ \leq 1.6\text{ V}$ (i.e., 1.5 VI/O) and $1.7\text{ V} \leq VDDQ \leq 1.95\text{ V}$ (i.e., 1.8 VI/O) and quoted at the worst case condition.

Power-up assumes: 1) linear ramp from 0V to VDD(MIN) within 200 ms
2) during ramp, $V_{IH} < VDD$ and $VDDQ < VDD$

Power supplies must be powered up simultaneously or else in the following sequence: VDD, VDDQ, VREF, followed by signal inputs. The power down sequence must be the reverse. VDDQ must not exceed VDD.

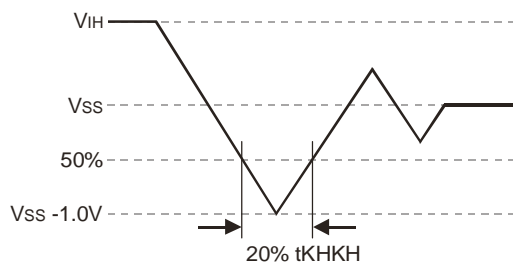
* VREF minimum is either 0.68 V or $0.46 * VDDQ$, whichever is larger.
VREF maximum is either 0.95 V or $0.54 * VDDQ$, whichever is smaller.

HSTL I/O Input Characteristics

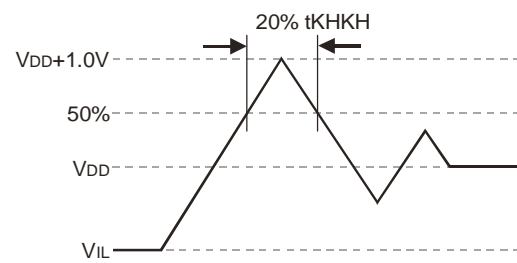
Parameter	Symbol	Min.	Max.	Unit	Notes
DC Input Logic High	V _{IH(DC)}	V _{REF} + 0.10	V _{DDQ} + 0.3	V	1, 2, 3
DC Input Logic Low	V _{IL(DC)}	-0.3	V _{REF} - 0.10	V	1, 2, 3
AC Input Logic High	V _{IH(AC)}	V _{REF} + 0.20	--	V	1, 5, 6
AC Input Logic Low	V _{IL(AC)}	--	V _{REF} - 0.20	V	1, 5, 6
V _{REF} Peak to Peak AC Voltage	V _{REF(AC)}	--	5% V _{REF(DC)}	V	4

- Compatible with both 1.8 V and 1.5 V I/O drivers.
- V_{IL(DC)} Min = -0.3 V, V_{IL(AC)} Min = -1.5 V (pulse width ≤ 3ns).
- V_{IH(DC)} Max = V_{DDQ} + 0.3 V, V_{IH(AC)} Max = V_{DDQ} + 0.85 V (pulse width ≤ 3ns).
- The peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
- To guarantee AC characteristics, V_{IL}, V_{IH}, Trise, and Tfall of inputs and clocks must be within 10% of each other.
- For devices supplied with HSTL I/O input buffers.

Undershoot/Overshoot Measurement and Timing



Undershoot



Overshoot

Capacitance

(TA = 25 °C, f = 1 MHz, V_{DD} = 1.8 V, V_{DDQ} = 1.5 V)

(These parameters tested initially and after any design or process change that may affect them)

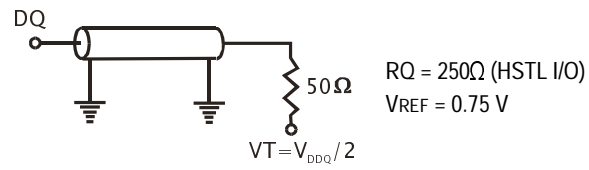
Parameter (sample tested)	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C _{IN}	V _{IN} = 0 V	4	5	pF
Output Capacitance	C _{OUT}	V _{OUT} = 0 V	6	7	pF
Clock Capacitance	C _{CLK}	--	5	6	pF

AC Test Conditions

Parameter	Conditions
Input high level	V _{DDQ}
Input low level	0 V
Maximum input slew rate	2 V/ns
Input reference level	V _{DDQ} /2
Output reference level	V _{DDQ} /2

Note: Test conditions specified with output loading as shown below unless otherwise noted.

AC Test Load Diagram



Input and Output Leakage Characteristics (μA)

Parameter	Symbol	Test Conditions	Min	Max
Input leakage current (except mode pins)	I_{IZ}	$V_{IN} = 0$ to V_{DDQ}	-2	2
Output leakage current	I_{OZ}	Output disable, $V_{OUT} = 0$ to V_{DDQ}	-2	2

Switching Characteristics (ns)

Parameter	Symbol	-333		-300		-267		-250		-200		-167		Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Clock														
K, \overline{K} Clock Cycle Time C, \overline{C} Clock Cycle Time	tKHKH tCHCH	3.0	3.5	3.3	4.2	3.75	5.5	4.0	6.3	5.0	7.88	6.0	8.4	
tKC Variance (Clock phase jitter)	tKCVar	--	0.2	--	0.2	--	0.2	--	0.2	--	0.2	--	0.2	5
K, \overline{K} Clock High Pulse Width C, \overline{C} Clock High Pulse Width	tKHKL tCHCL	1.2	--	1.32	--	1.6	--	1.6	--	2.0	--	2.4	--	
K, \overline{K} Clock Low Pulse Width C, \overline{C} Clock Low Pulse Width	tKLKH tLCLH	1.2	--	1.32	--	1.6	--	1.6	--	2.0	--	2.4	--	
K to \overline{K} High C to \overline{C} High	tKH \overline{KH} tCH \overline{CH}	1.35	--	1.49	--	1.8	--	1.8	--	2.2	--	2.7	--	
K, \overline{K} Clock High to C, \overline{C} Clock High	tKHCH	0	1.3	0	1.45	0	1.8	0	1.8	0	2.3	0	2.8	
K Static to DLL reset	tKCRreset	30	--	30	--	30	--	30	--	30	--	30	--	
Output Times														
K, \overline{K} Clock High to Data Output Valid C, \overline{C} Clock High to Data Output Valid	tKHQV tCHQV	--	0.45	--	0.45	--	0.45	--	0.45	--	0.45	--	0.5	3
K, \overline{K} Clock High to Data Output Hold C, \overline{C} Clock High to Data Output Hold	tKHQX tCHQX	-0.45	--	-0.45	--	-0.45	--	-0.45	--	-0.45	--	-0.5	--	3
K, \overline{K} Clock High to Echo Clock Valid C, \overline{C} Clock High to Echo Clock Valid	tKHQCV tCHQCV	--	0.45	--	0.45	--	0.45	--	0.45	--	0.45	--	0.5	
K, \overline{K} Clock High to Echo Clock Hold C, \overline{C} Clock High to Echo Clock Hold	tKHQCX tCHQCX	-0.45	--	-0.45	--	-0.45	--	-0.45	--	-0.45	--	-0.5	--	
CQ, \overline{CQ} High Output Valid	tCQHCV	--	0.25	--	0.27	--	0.30	--	0.30	--	0.35	--	0.40	7
CQ, \overline{CQ} High Output Hold	tCQHCV	0.25	--	0.27	--	0.30	--	0.30	--	0.35	--	0.40	--	7
K Clock High to Data Output High-Z C Clock High to Data Output High-Z	tKHQZ tCHQZ	--	0.45	--	0.45	--	0.45	--	0.45	--	0.45	--	0.5	3
K Clock High to Data Output Low-Z C Clock High to Data Output Low-Z	tKHQX1 tCHQX1	-0.45	--	-0.45	--	-0.45	--	-0.45	--	-0.45	--	-0.5	--	3
Setup Times														
Address Input Setup Time	tAVKH	0.4	--	0.4	--	0.5	--	0.5	--	0.6	--	0.7	--	
Control Input Setup Time	tIVKH	0.4	--	0.4	--	0.5	--	0.5	--	0.6	--	0.7	--	2
Data Input Setup Time	tDVKH	0.28	--	0.3	--	0.35	--	0.35	--	0.4	--	0.5	--	
Hold Times														
Address Input Hold Time	tKHAX	0.4	--	0.4	--	0.5	--	0.5	--	0.6	--	0.7	--	
Control Input Hold Time	tKHIX	0.4	--	0.4	--	0.5	--	0.5	--	0.6	--	0.7	--	
Data Input Hold Time	tKHDX	0.28	--	0.3	--	0.35	--	0.35	--	0.4	--	0.5	--	

Notes:

1. All Address inputs must meet the specified setup and hold times for all latching clock edges.
2. Control signals are R/\overline{W} and $\overline{B\overline{W}n}$.
3. If C clocks are tied high, K clocks become the references for C clock timing parameters.

- To avoid bus contention, at any given voltage and temperature tCHQX1 is bigger than tCHQZ. The specs as shown do not imply bus contention because tCHQX1 is a MIN parameter that is worst case at totally different test conditions (0°C, 1.9 V) than tCHQZ, which is a MAX parameter (worst case at 70°C, 1.7 V). It is not possible for two RAMs on the same board to be at such different voltages and temperatures.
- Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
- DLL Lock Time (tKClock) is a minimum of 1024 cycles in all cases. VDD slew rate must be less than 0.1 V DC per 50ns for DLL lock retention. DLL lock time begins once VDD and input clock are stable.
- Echo clock is very tightly controlled to data valid/data hold. By design, there is a ±0.1 ns variation from echo clock to data. The datasheet parameters reflect tester guard bands and test setup variations.

Programmable Impedance HSTL Output Driver DC Electrical Characteristics (V)

Parameter	Symbol	Condition	Min	Max	Notes
Output High Voltage	VOH	RQ = 250• and VDDQ = 1.5 V or 1.8 V	VDDQ/2	VDDQ	1
		Minimum Impedance mode, ZQ = Vss	VDDQ – 0.2	VDDQ	2
Output Low Voltage	VOL	RQ = 250• and VDDQ = 1.5 V or 1.8 V	Vss	VDDQ/2	3
		Minimum Impedance mode, ZQ = Vss	Vss	0.2	4

Notes:

- $I_{OH} = - (V_{DDQ}/2) / (RQ/5) \pm 15\%$ @ $V_{OH} = V_{DDQ}/2$ (for: $175\Omega \leq RQ \leq 350\Omega$).
- $I_{OH} = -1.0$ mA, nominal impedance
- $I_{OL} = (V_{DDQ}/2) / (RQ/5) \pm 15\%$ @ $V_{OL} = V_{DDQ}/2$ (for: $175\Omega \leq RQ \leq 350\Omega$).
- $I_{OL} = 1.0$ mA, nominal impedance

Operating Currents (DDR)

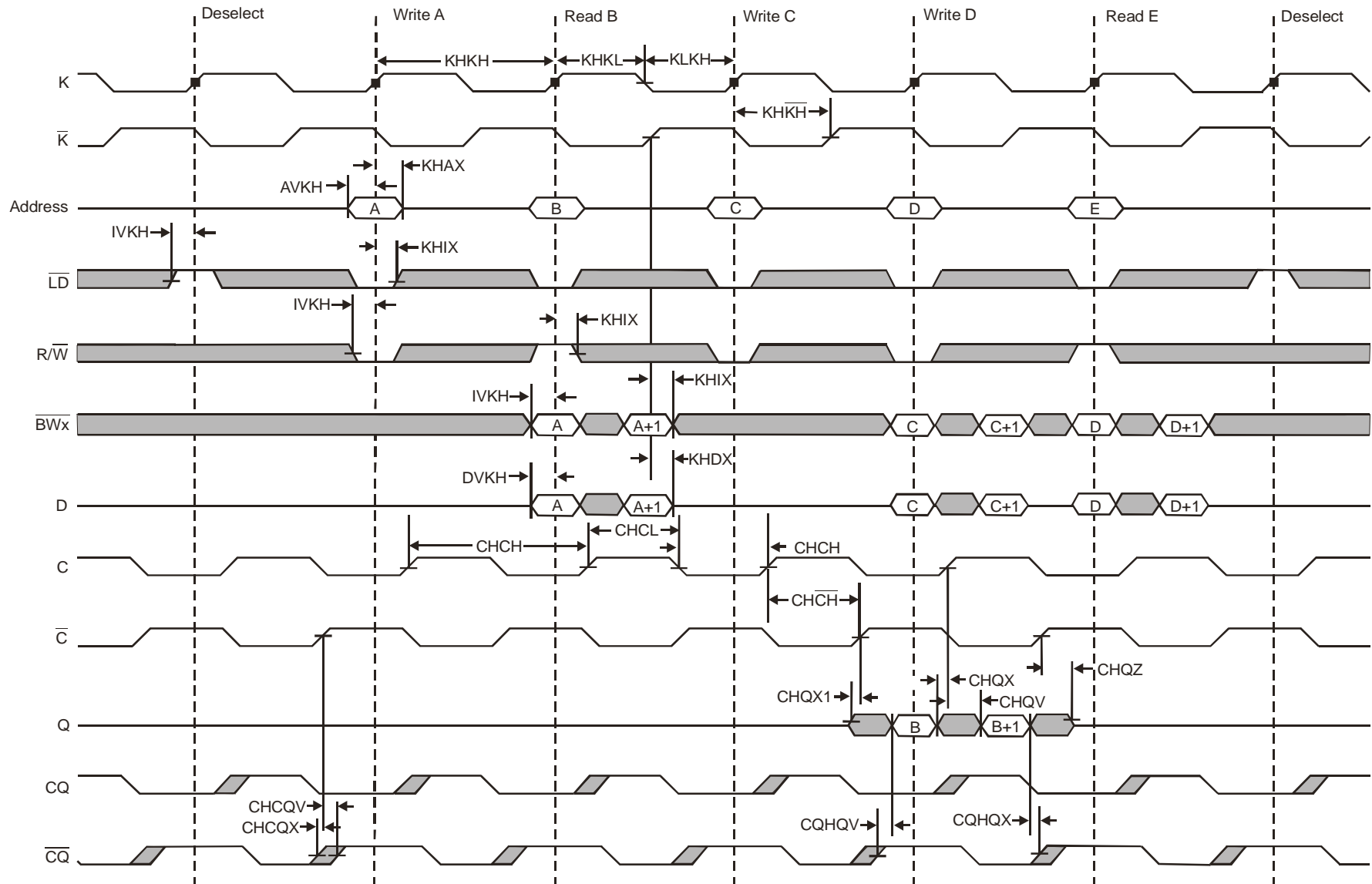
Parameter	Test Conditions	Symbol	-333		-300		-267		-250		-200		-167	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
x36 Operating Current	VDD = max, IOUT = 0 mA Cycle time • tKHKH Min	IDD	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
x18 Operating Current			tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
x9 Operating Current			tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
Standby Current (NOP)	Device deselected, IOUT = 0 mA, f = max, Inputs • 0.2 V or • VDD – 0.2V	ISB1	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd

Notes:

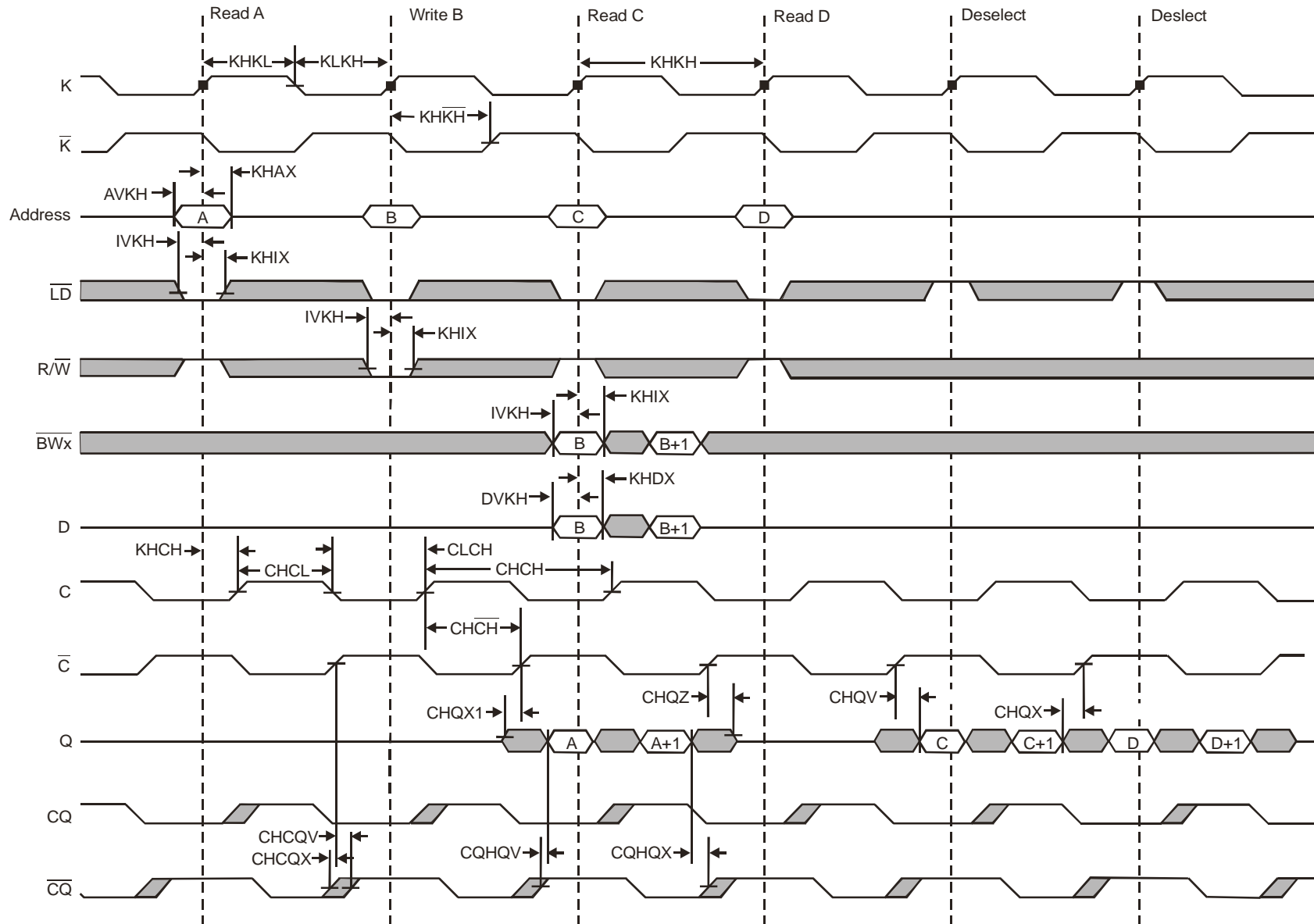
- Power measured with output pins floating.
- Minimum cycle, IOUT = 0 mA
- Operating current is calculated with 50% read cycles and 50% write cycles.
- Standby Current is only after all pending read and write burst operations are completed.

Timing Diagrams

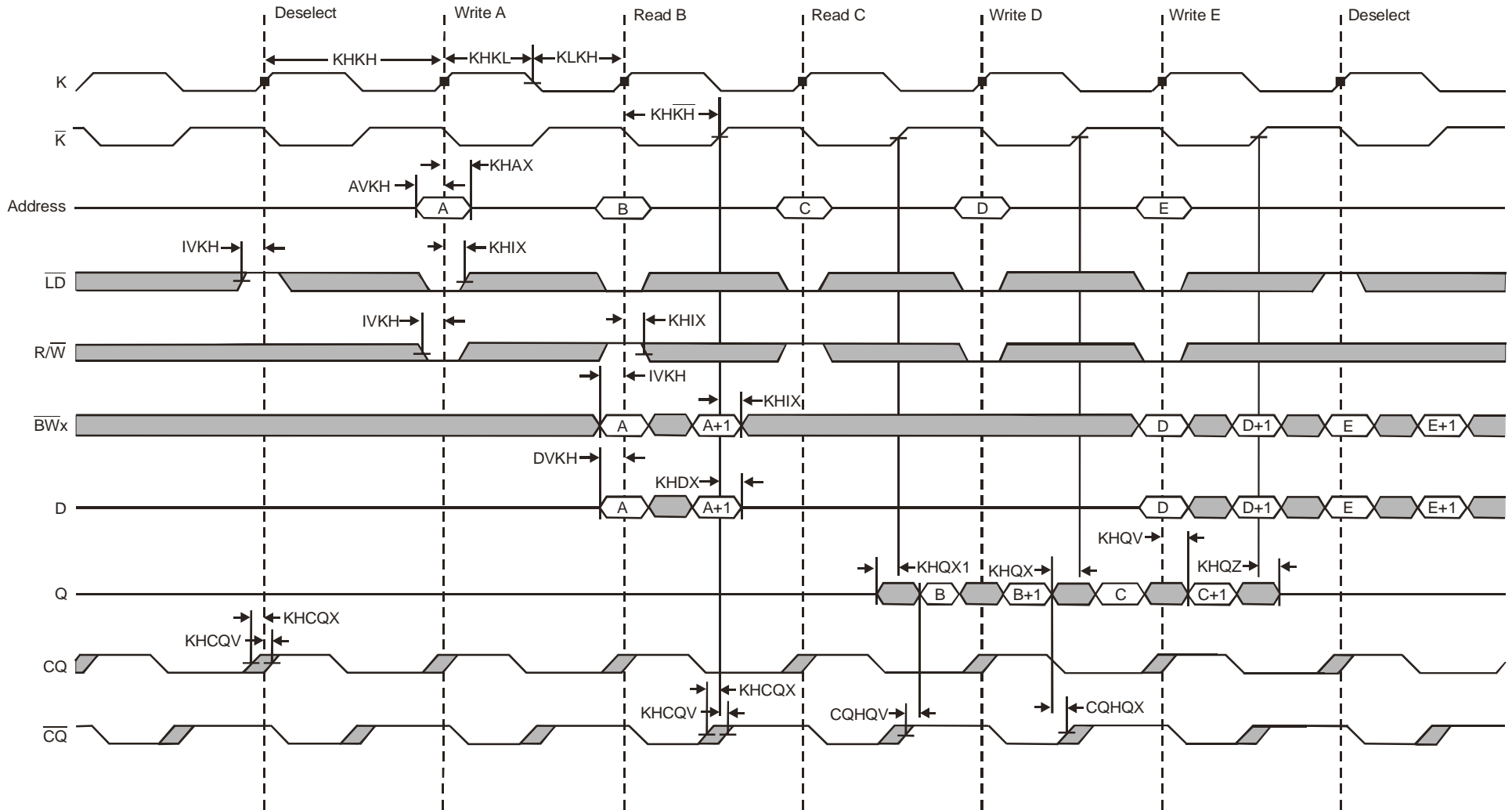
C and \bar{C} Controlled Write-First



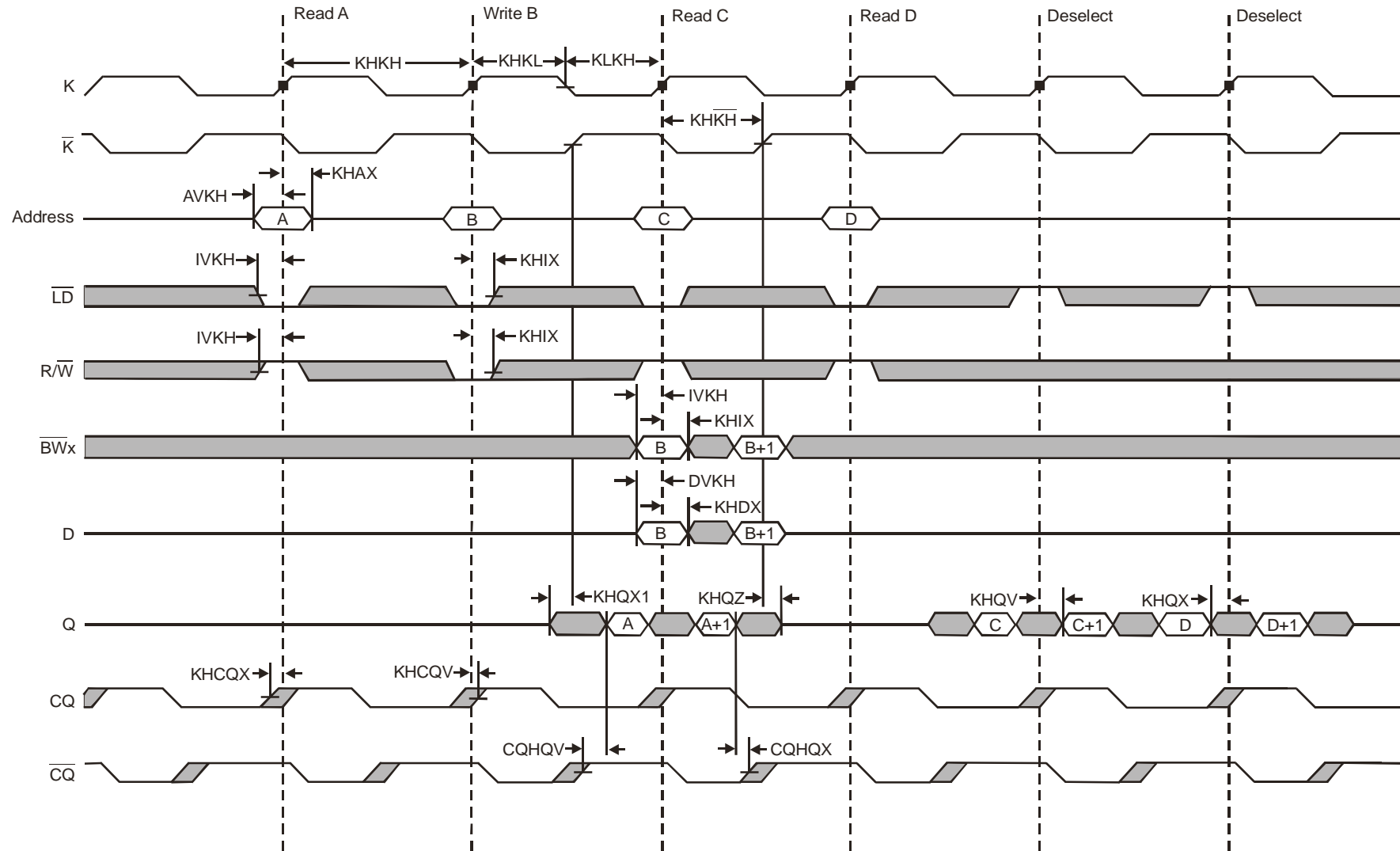
C and \bar{C} Controlled Read-First



K and \bar{K} Controlled Write-First



K and \bar{K} Controlled Read-First



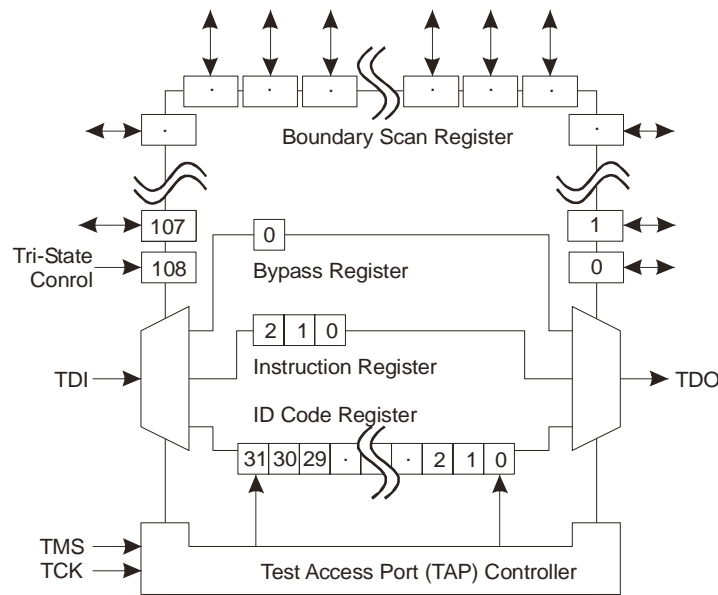
JTAG Port Operation

Overview

This device incorporates a serial boundary scan interface that complies with IEEE Standard 1149.1-1990, commonly known as JTAG. The JTAG Port is also known as a Test Access Port, or TAP. It can be used to read the device ID code, monitor all RAM input and I/O pads, drive pre-loaded values into the I/O bus, or the I/O bus to a High-Z state.

The port's input interface levels scale with VDD and the output drivers are powered by VDDQ. The port is reset at power-up and remains inactive until clocked. Pins, registers, states, and instructions are described below.

JTAG Test Access Port Block Diagram



JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all events. Inputs are captured on the rising edge; outputs are driven on the falling edge.
TMS	Test Mode Select	In	Command input for the JTAG state machine, sampled on the rising edge of TCK.
TDI	Test Data In	In	The input side of any selected register, sampled on the rising edge of TCK.
TDO	Test Data Out	Out	The output side of any selected register, driven on the falling edge of TCK.

Notes: TCK, TDI, and TMS have internal pull-up circuits; when undriven they produce a logic one input level.

This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The JTAG controller is reset automatically at power-up, and again whenever it enters the Test-Logic-Reset state.

The "selected" register is determined by the current instruction and the state of the JTAG controller.

Disabling the JTAG Port

For normal operation of the device without using JTAG, the controller can be held in a permanent Reset state. To do this, TCK, TDI, and TMS are left floating or tied to either VDD or VSS. TDO should be left unconnected.

JTAG Registers

The JTAG interface has four serial shift registers that are used in conjunction with JTAG instructions. When a register is selected, it is placed between TDI and TDO so that it can shift data out serially on the falling edges of TCK and capture input data on the rising edges of TCK, depending on the state of the controller.

Instruction Register

The three-bit Instruction Register holds an instruction to be executed. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller enters the Test-Logic-Reset state. The user may load instructions through the TDI pin using the various IR (Instruction Register) states. The Instruction Register is always selected in the IR states, regardless of the current instruction.

Bypass Register

The single-bit Bypass Register can be placed between TDI and TDO to pass serial data through the JTAG Port with as little delay as possible. The Bypass Register is selected by the BYPASS instruction.

Identification (ID) Register

The 32-bit ID Register receives an identification code from an on-chip ID ROM. The code describes various attributes of the RAM as indicated in the table below. The ID Register is selected by the IDCODE instruction.

ID Code Contents

	Die Revision Code				Not Used								I/O Configuration								Tezzaron Semiconductor JEDEC Vendor ID Code								Presence Register				
Bit#	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
x36	X	X	X	X	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1
x16	X	X	X	X	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	1	0	1	1	0	0	1	
x9	X	X	X	X	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	1	0	0	0	0	0	1	0	1	1	0	0	1	

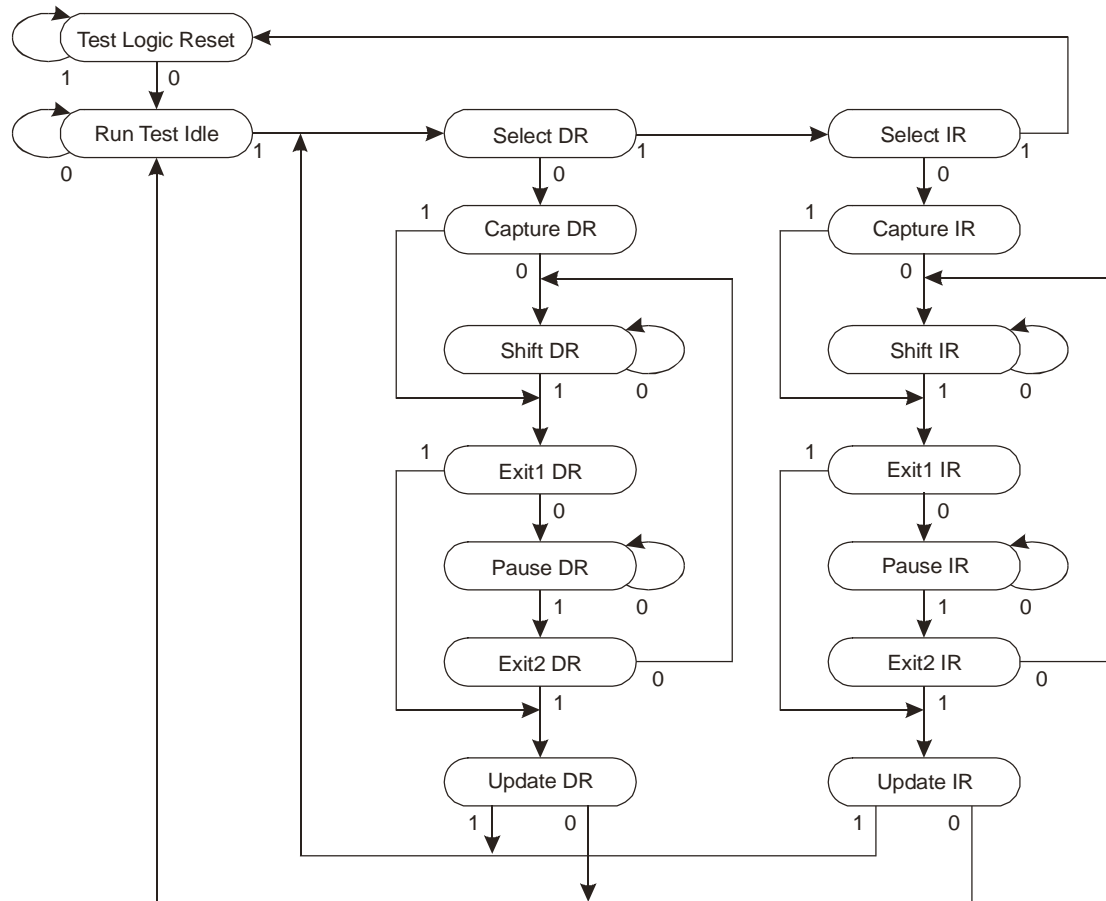
Boundary Scan Register

The Boundary Scan Register is a chain of 109 cells. Each cell contains a Scan bit and an Update bit. The Scan bits can capture the logic level found on the RAM's I/O pins; the Update bits can drive a preloaded set of data onto the RAM's outputs. The Boundary Scan Register cells are daisy chained together so their contents can be shifted out serially through the TDO pin and loaded through the TDI pin. The relationship between the device pins and the cells in the Boundary Scan Register is described in the Scan Order Table below; note that the register includes a number of special purpose cells that do not represent I/O pins. The Boundary Scan Register is selected by the SAMPLE-Z, SAMPLE/PRELOAD, and EXTEST instructions.

Scan Order Table

Cell#	Pin Name	I/O	Notes	Cell#	Pin Name	I/O	Notes	Cell#	Pin Name	I/O	Notes	Cell#	Pin Name	I/O	Notes
0	tbd	tbd		28	tbd	tbd		56	tbd	tbd		84	tbd	tbd	
1	tbd	tbd		29	tbd	tbd		57	tbd	tbd		85	tbd	tbd	
2	tbd	tbd		30	tbd	tbd		58	tbd	tbd		86	tbd	tbd	
3	tdb	tbd		31	tdb	tbd		59	tdb	tbd		87	tdb	tbd	
4	tbd	tbd		32	tbd	tbd		60	tbd	tbd		88	tbd	tbd	
5	tbd	tbd		33	tbd	tbd		61	tbd	tbd		89	tbd	tbd	
6	tbd	tbd		34	tbd	tbd		62	tbd	tbd		90	tbd	tbd	
7	tdb	tbd		35	tdb	tbd		63	tdb	tbd		91	tdb	tbd	
8	tdb	tdb		36	tdb	tdb		64	tdb	tdb		92	tdb	tdb	
9	tdb	tdb		37	tdb	tdb		65	tdb	tdb		93	tdb	tdb	
10	tdb	tdb		38	tdb	tdb		66	tdb	tdb		94	tdb	tdb	
11	tdb	tdb		39	tdb	tdb		67	tdb	tdb		95	tdb	tdb	
12	tdb	tdb		40	tdb	tdb		68	tdb	tdb		96	tdb	tdb	
13	tdb	tdb		41	tdb	tdb		69	tdb	tdb		97	tdb	tdb	
14	tdb	tdb		42	tdb	tdb		70	tdb	tdb		98	tdb	tdb	
15	tdb	tdb		43	tdb	tdb		71	tdb	tdb		99	tdb	tdb	
16	tdb	tdb		44	tdb	tdb		72	tdb	tdb		100	tdb	tdb	
17	tdb	tdb		45	tdb	tdb		73	tdb	tdb		101	tdb	tdb	
18	tdb	tdb		46	tdb	tdb		74	tdb	tdb		102	tdb	tdb	
19	tdb	tdb		47	tdb	tdb		75	tdb	tdb		103	tdb	tdb	
20	tdb	tdb		48	tdb	tdb		76	tdb	tdb		104	tdb	tdb	
21	tdb	tdb		49	tdb	tdb		77	tdb	tdb		105	tdb	tdb	
22	tdb	tdb		50	tdb	tdb		78	tdb	tdb		106	tdb	tdb	
23	tdb	tdb		51	tdb	tdb		79	tdb	tdb		107	tdb	tdb	
24	tdb	tdb		52	tdb	tdb		80	tdb	tdb		108	Tri-State Control	n/a	
25	tdb	tdb		53	tdb	tdb		81	tdb	tdb					
26	tdb	tdb		54	tdb	tdb		82	tdb	tdb					
27	tdb	tdb		55	tdb	tdb		83	tdb	tdb					

JTAG Controller State Diagram



JTAG Controller States

Overview

The JTAG controller is inactive until clocked with TCK. When TCK is activated, the controller is in the Test Logic Reset state. Subsequent transitions between states are controlled by the TMS signal as shown in the diagram above. TMS is sampled at each rising edge of TCK.

The DR states select and manipulate the four JTAG data registers; the IR states select and manipulate the Instruction Register.

Test Logic Reset

In this state, the IDCODE instruction is loaded into the Instruction Register, no control is exerted over the RAM's output pins, and the RAM executes as if the JTAG port were disabled. If TMS is held at 1 for five cycles, the controller returns to this state and loops until it detects a TMS value of 0.

Run Test Idle

This is the entry point for all instructions. The controller can loop here as needed, but performs no functions.

Select DR

The controller selects a data register (determined by the current instruction) and places it between TDI and TDO.

Capture DR

Depending upon the current instruction, the selected register may receive data from sources other than TDI.

Shift DR

On the falling edge of TCK, the least significant bit of the selected register is shifted onto TDO. On the rising edge of TCK, the value on the TDI pin is captured and shifted into the most significant bit of the selected register.

Exit1 DR

Data movement stops. No function is performed.

Pause DR

The controller can loop here, but performs no functions.

Exit2 DR

No function is performed.

Update DR

If the current instruction is SAMPLE or EXTEST, data in the Boundary Scan Register is copied from the Scan bits to the Update bits. Otherwise, no function is performed.

Select IR

The Instruction Register is selected and placed between TDI and TDO.

Capture IR

The controller loads the two least significant bits of the Instruction Register with 01.

Shift IR, Exit1 IR, Pause IR, Exit2 IR

These states are analogous to Shift DR, Exit1 DR, Pause DR, and Exit2 DR.

Update IR

Instruction loading is complete; the instruction is decoded for implementation. If the new instruction is EXTEST or SAMPLE-Z, JTAG exerts control over the RAM's output pins; otherwise, it releases control of those pins.

JTAG Controller Instruction Set

Instruction Summary

Instruction	Binary Code	Description
EXTEST	000	Either drives contents onto RAM outputs or forces outputs to High-Z; selects Boundary Scan Register; captures I/O ring contents; allows reading/loading of Boundary Scan Register.
IDCODE	001	Selects and loads ID Register; allows reading of register. Default instruction – automatically loaded in test-logic-reset state.
SAMPLE-Z	010	Forces all RAM outputs to High-Z; selects Boundary Scan Register; captures I/O ring contents; allows reading of Boundary Scan Register.
RFU	011	Do not use this instruction; reserved for future use. (Currently replicates BYPASS instruction.)
SAMPLE/PRELOAD	100	Selects Boundary Scan Register; captures I/O ring contents; allows reading/loading of Boundary Scan Register.
TEZZARON	101	Tezzaron private instruction; do not use.
RFU	110	Do not use this instruction; Reserved for Future Use. (Currently replicates BYPASS instruction.)
BYPASS	111	Selects Bypass Register; allows rapid pass-through of data.

Instruction Descriptions

NOTE: Several of these instructions capture signals from the RAM's I/O ring. The user must be aware that the JTAG clock (TCK) operates at 20 MHz or less, while the RAM clock operates more than an order of magnitude faster. Because of the difference in clock frequencies, it is possible that an input or output will undergo a transition during the capture. In this case, the signal may be captured while in transition. This will not harm the device, but there is no guarantee as to the value that will be captured, and repeatable results may not be possible. To guarantee that the correct value of a signal is captured, the signal must be stabilized long enough to meet the JTAG set-up plus hold times ($t_{TS} + t_{TH}$). If there is no way in a design to stop (or slow) the RAM clock, the RAM clock inputs might not be captured correctly; however, it is still possible to capture all other signals and simply ignore the captured values of the RAM clock signals.

BYPASS

This instruction allows test data to pass through the device with minimal delay, to facilitate testing of other devices on the scan path.

Select-DR: The Bypass Register is placed between TDI and TDO.

Shift-DR: Data is shifted out through TDO and in from TDI.

SAMPLE/PRELOAD

This instruction allows sample data to be captured and examined without interfering with normal device operation. It also allows test data to be pre-loaded for later use with the EXTEST instruction.

Select-DR: The Boundary Scan Register is placed between TDI and TDO.

Capture-DR: A snapshot of data from all the RAM's I/O pins is captured in the Scan bits of the cells.

Shift-DR: Data in the Scan bits is shifted out serially through TDO and data presented to TDI is shifted in.

Update-DR: Data from the Scan bits is copied into the Update bits for later use (see EXTEST).

EXTEST

This instruction captures sample data and sets up test data, much like SAMPLE/PRELOAD, but it also controls the RAM's output pins. EXTEST is for testing only, as it will disrupt normal operation of the device. As soon as the EXTEST instruction is loaded (in Update-IR), it exerts control over the RAM's output pins and does not release them until a new instruction is loaded. The values in the Boundary Scan Register's Update bits are driven onto the output pins, *unless the Tri-State Control cell has been set (see below)*, in which case the output pins are tri-stated.

EXTEST and Tri-State

The Boundary Scan Register's last cell, #108, is the Tri-State Control cell. During EXTEST, it directly controls the state of the RAM's output pins. When HIGH, it enables the Update bit values to drive the output bus; when LOW, it places the output bus into a High-Z condition. The Tri-State Control cell's value is set to HIGH whenever the controller is in the "Test-Logic-Reset" state. The value is changed with the SAMPLE/PRELOAD or EXTEST instruction by shifting the desired value into the cell during the Shift-DR state. During Update-DR, the new value is copied into the cell's Update bit. From there, it controls the EXTEST instruction's behavior.

Select-DR: The Boundary Scan Register is placed between TDI and TDO.

Capture-DR: A snapshot of data from all the RAM's I/O pins is captured in the Scan bits of the cells.

Shift-DR: Data in the Scan bits is shifted out serially through TDO and data presented to TDI is shifted in.

Update-DR: Data in the Scan bits is copied to the Update bits. The values take effect immediately, driving the RAM's output bus as directed.

IDCODE

IDCODE is the default instruction, loaded automatically whenever the controller is placed in the Test-Logic-Reset state. It allows access to the device's internal ID ROM contents.

Select-DR: The ID Register is placed between TDI and TDO.

Capture-DR: The ID Register is loaded with the device's 32-bit identification code from the ID ROM.

Shift-DR: The contents of the ID Register is shifted out through TDO.

SAMPLE-Z

This instruction functions somewhat like EXTEST, except that the output bus is always tri-stated and the Update bits are not changed. Like EXTEST, it is disruptive to normal device operation. As soon as the SAMPLE-Z instruction is loaded (in Update-IR), it exerts control over the RAM's output pins and does not release them until a new instruction is loaded.

Select-DR: The Boundary Scan Register is connected between TDI and TDO.

Capture-DR: A snapshot of data from all the RAM's I/O pins is captured in the Scan bits.

Shift-DR: Data in the Scan bits is shifted out serially through TDO.

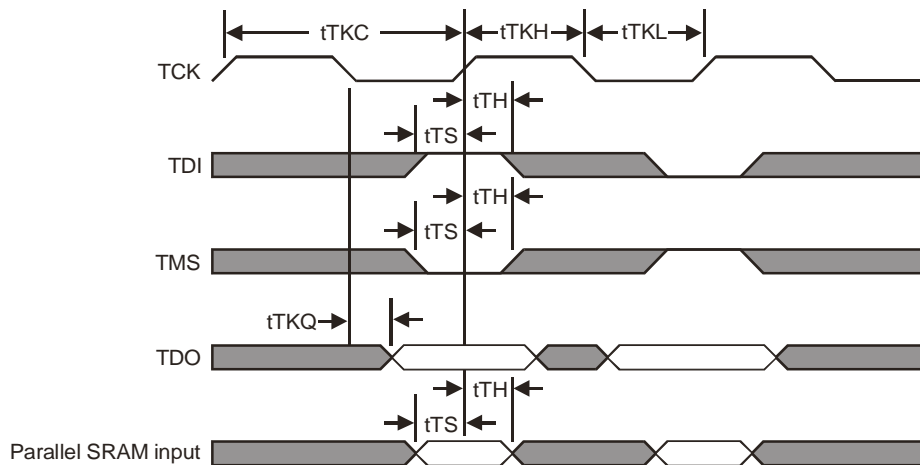
Tezzaron

This instruction is reserved for vendor use; do not use.

RFU

This instruction is reserved for future use; in this device it replicates the BYPASS instruction.

JTAG Port Timing Diagram



JTAG Port Recommended Operating Conditions and DC Characteristics (V)

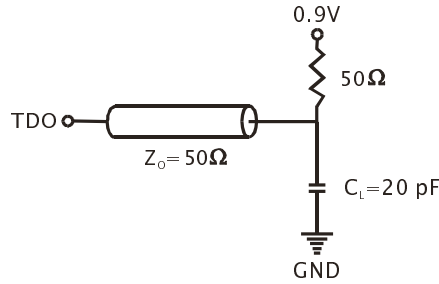
Parameter	Symbol	Min.	Typ.	Max.
Power Supply Voltage	V _{DDQ}	1.7	1.8	1.9
Input High Voltage	V _{IH}	1.3	--	V _{DD} + 0.3
Input Low Voltage	V _{IL}	-0.3	--	0.5
Output High Voltage (I _{OH} = -2 mA)	V _{OH}	1.4	--	V _{DD}
Output Low Voltage (I _{OL} = 2 mA)	V _{OL}	V _{SS}	--	0.4

Note: During JTAG operation, the input level of the RAM pins must conform to the device's DC specifications.

JTAG Port AC Test Conditions

Parameter	Symbol	Min	Unit
Input High/Low Level	V _{IH} /V _{IL}	1.3/0.5	V
Input Rise/Fall Time	T _R /T _F	1.0/1.0	ns
Input and Output Timing Reference Level	--	0.9	V

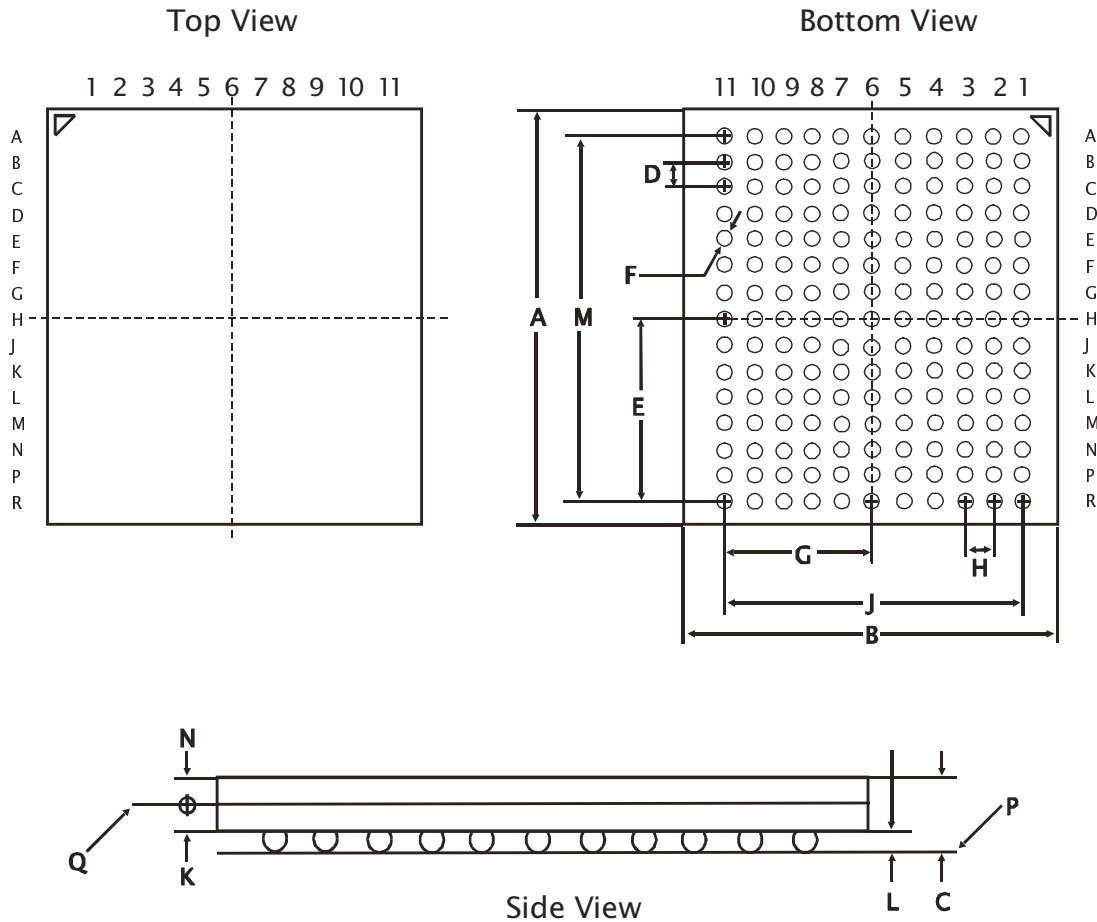
Parameters are measured with distributed scope and test jig capacitance.
Conditions as shown in diagram below unless otherwise noted.



JTAG Port AC Electrical Characteristics (ns)

Parameter	Symbol	Min	Max
TCK Cycle Time	tTKC	50	—
TCK High Pulse Width	tTKH	20	—
TCK Low Pulse Width	tTKL	20	—
Set Up Time – (TDI, TMS, Capture)	tTS	5	—
Hold Time – (TDI, TMS, Capture)	tTH	5	—
TCK Low to TDO Valid	tTKQ	0	10

Package Drawing



Symbol	Description	Measurement (mm)
A	Chip Length	17.00±0.10
B	Chip Width	15.00±0.10
C	Chip Height	1.40 max.
D	Length between pin centers	1.00
E	Length between center pin and outermost pin	7.00
F	Pin diameter	0.50 +0.14 / -0.06
G	Width between center pin and outermost pin	5.00
H	Width between pin centers	1.00
J	Width between outermost pins	10.00
K	Height of circuit card	0.36
L	Height of pins	0.35±0.06

Symbol	Description	Measurement (mm)
M	Length between outermost pins	14.00
N	Height of encapsulant	0.53±0.05
P	Seating Plane *	
Q	Top Plane of circuit card **	

Pin centers: within 0.05 mm of relative position at MMC
Pin centers: within 0.25 mm of true position at MMC
Package length/width edges: uniform within 0.15 mm
Package weight: tbd
Solder pad type NSMD (non-solder mask defined)
JEDEC reference: MO-216 – design 4.6C

* Seating plane surface uniform within 0.15 mm

** Top plane parallel to seating plane within 0.25 mm

Document History

Datasheet for TSC3D272S09 / 18 / 36

Revision	Date	Changes
1.0	24 January 2007	Original

Document Contents

Features.....	1
Functional Description	1
Pin Configurations	2
2M x 36: Top View	2
4M x 18: Top View	3
8M x 9: Top View	4
Pin Descriptions.....	5
Functional Details	5
Clocks	5
Burst Operations	5
Read and Write Ports.....	5
Read Cycles.....	6
Write Cycles.....	6
Power-Up Sequence.....	6
DLL Constraints	6
Power-Up Sequence ($\overline{\text{Doff}}$ Controlled).....	7
Power-Up Sequence ($\overline{\text{Doff}}$ Tied High).....	7
Byte Write Control.....	7
Example: x18 Write Sequence Using Byte Write Enables	7
Output Register Control	8
Output Driver Impedance Control	8
Truth Tables.....	8
I/O Truth Table.....	8
Byte Write Enable Truth Table, x18	8
Byte Write Enable Truth Table, x36	9
State Diagram.....	9
Electrical Characteristics	10
Absolute Maximum Ratings	10
Recommended Operating Conditions.....	10
HSTL I/O Input Characteristics	11
Undershoot/Overshoot Measurement and Timing.....	11
Capacitance	11
AC Test Conditions	11
AC Test Load Diagram	12
Input and Output Leakage Characteristics (μA).....	12
Switching Characteristics (ns).....	13
Programmable Impedance HSTL Output Driver DC Electrical Characteristics (V)	14

Operating Currents (DDR)	14
Timing Diagrams.....	15
C and \bar{C} Controlled Write-First	15
C and \bar{C} Controlled Read-First	16
K and \bar{K} Controlled Write-First	17
K and \bar{K} Controlled Read-First.....	18
JTAG Port Operation	19
Package Drawing.....	27
Document History	28
Document Contents	28