72Mb Synchronous Quad Transfer Rate (QTRII™) 3T-iRAM™

Burst of 2
SRAM-Compatible

Features

- Error-resistant 3T-iRAM™ technology
- Dual DDRII Interface
- Pin-compatible with QDRII™ and SigmaQuad-II™ SRAMs
- JEDEC-standard pinout and package
- Burst of 2 Read and Write
- Separate independent Read and Write data ports
- Concurrent Read/Write transactions are supported
- Separate Port Selects for depth expansion
- Synchronous internally self-timed Writes
- 1.8 V +100/–100 mV core power supply
- Expanded HSTL output voltage: 1.4 V to 1.9 V
- Fully coherent read and write pipelines
- ZQ pin for programmable output drive strength
- IEEE 1149.1 JTAG-compliant Boundary Scan
- 165-bump 15mm x 17mm BGA, 1 mm bump pitch
- Pin-compatible with 9Mb, 18Mb, 36Mb, and 144Mb devices

Options / Marking

Options		Marking
Configurations:	8M x 9	S09
	4M x 18	S18
	2M x 36	S36
Package:	165 FBGA	B
Speed (MHz):	333 MHz	-333
	300 MHz	-300
	267 MHz	-267
	250 MHz	-250
	200 MHz	-200
	167 MHz	-167

- Part number example: **TSC3Q272S18B-300**

Functional Description

3T-iRAM™ is a unique type of dynamic memory. Tezzaron has crafted these pseudo-static devices to provide entirely SRAM-compatible interfaces and timing. The unique design of these 3T memories provides soft error rates up to 10 times lower than equivalent high-speed, high-density SRAMs, while maintaining drop-in compatibility.

QTRII™ (Quad Transfer Rate II) is a Separate I/O architecture that makes these devices drop-in compatible with QDRII™ and SigmaQuad-II™ SRAMs. It accesses the memory array with two separate ports for Read and Write operations, using dedicated data input and output pins and a common address bus. This completely eliminates the “bus turn-around” time required in Common I/O devices. To maximize throughput, both data ports use DTRII™ (Double Transfer Rate II) interfaces.

These pipelined synchronous 72Mb devices employ two input register clocks, K and $\overline{K}$. The user can manipulate the output register clocks quasi-independently with C and $\overline{C}$. All four of these clocks are independent single-ended clock inputs, not differential inputs, for precise data timing. If the C clocks are tied high, the K clocks are routed internally to fire the output registers instead.

These devices always transfer data in two packets. A0 is internally set to 0 for the first data transfer of a burst and automatically incremented to 1 for the second transfer.

Speed Parameter Synopsis:
(all units ns)

	-333	-300	-267	-250	-200	-167
tKHKH	3.00	3.30	3.75	4.00	5.00	6.00
tKHQV	0.45	0.45	0.45	0.45	0.45	0.50

2M x 36: Top View

11 x 15 Bump BGA – 15 x 17 mm2 Body – 1 mm Bump Pitch

	1	2	3	4	5	6	7	8	9	10	11	
A	$\overline{CQ}$	VSS/288M	SA	$\overline{W}$	$\overline{BW2}$	$\overline{K}$	$\overline{BW1}$	$\overline{R}$	SA	VSS/144M	CQ	A
B	Q27	Q18	D18	SA	$\overline{BW3}$	K	$\overline{BW0}$	SA	D17	Q17	Q8	B
C	D27	Q28	D19	VSS	SA	SA	SA	VSS	D16	Q7	D8	C
D	D28	D20	Q19	VSS	VSS	VSS	VSS	VSS	Q16	D15	D7	D
E	Q29	D29	Q20	VDDQ	VSS	VSS	VSS	VDDQ	Q15	D6	Q6	E
F	Q30	Q21	D21	VDDQ	VDD	VSS	VDD	VDDQ	D14	Q14	Q5	F
G	D30	D22	Q22	VDDQ	VDD	VSS	VDD	VDDQ	Q13	D13	D5	G
H	$\overline{Doff}$	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ	H
J	D31	Q31	D23	VDDQ	VDD	VSS	VDD	VDDQ	D12	Q4	D4	J
K	Q32	D32	Q23	VDDQ	VDD	VSS	VDD	VDDQ	Q12	D3	Q3	K
L	Q33	Q24	D24	VDDQ	VSS	VSS	VSS	VDDQ	D11	Q11	Q2	L
M	D33	Q34	D25	VSS	VSS	VSS	VSS	VSS	D10	Q1	D2	M
N	D34	D26	Q25	VSS	SA	SA	SA	VSS	Q10	D9	D1	N
P	Q35	D35	Q26	SA	SA	C	SA	SA	Q9	D0	Q0	P
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI	R

Notes: $\overline{BW0}$ controls writes to D0:D8
$\overline{BW1}$ controls writes to D9:D17
$\overline{BW2}$ controls writes to D18:D26
$\overline{BW3}$ controls writes to D27:D35

4M x 18: Top View

11 x 15 Bump BGA – 15 x 17 mm2 Body – 1 mm Bump Pitch

	1	2	3	4	5	6	7	8	9	10	11	
A	$\overline{CQ}$	VSS/144M	SA	$\overline{W}$	$\overline{BW1}$	$\overline{K}$	NC	$\overline{R}$	SA	SA	CQ	A
B	NC	Q9	D9	SA	NC	K	$\overline{BW0}$	SA	NC	NC	Q8	B
C	NC	NC	D10	VSS	SA	SA	SA	VSS	NC	Q7	D8	C
D	NC	D11	Q10	VSS	VSS	VSS	VSS	VSS	NC	NC	D7	D
E	NC	NC	Q11	VDDQ	VSS	VSS	VSS	VDDQ	NC	D6	Q6	E
F	NC	Q12	D12	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	Q5	F
G	NC	D13	Q13	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	D5	G
H	$\overline{Doff}$	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ	H
J	NC	NC	D14	VDDQ	VDD	VSS	VDD	VDDQ	NC	Q4	D4	J
K	NC	NC	Q14	VDDQ	VDD	VSS	VDD	VDDQ	NC	D3	Q3	K
L	NC	Q15	D15	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	Q2	L
M	NC	NC	D16	VSS	VSS	VSS	VSS	VSS	NC	Q1	D2	M
N	NC	D17	Q16	VSS	SA	SA	SA	VSS	NC	NC	D1	N
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0	P
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI	R

Notes: $\overline{BW0}$ controls writes to D0:D8
$\overline{BW1}$ controls writes to D9:D17

8M x 9: Top View

11 x 15 Bump BGA – 15 x 17mm2 Body – 1 mm Bump Pitch

	1	2	3	4	5	6	7	8	9	10	11	
A	$\overline{CQ}$	SA	SA	$\overline{W}$	NC	$\overline{K}$	NC	$\overline{R}$	SA	SA	CQ	A
B	NC	NC	NC	SA	NC	K	$\overline{BW}$	SA	NC	NC	Q4	B
C	NC	NC	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	D4	C
D	NC	D5	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC	D
E	NC	NC	Q5	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D3	Q3	E
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC	F
G	NC	D6	Q6	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC	G
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ	H
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q2	D2	J
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC	K
L	NC	Q7	D7	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q1	L
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D1	M
N	NC	D8	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC	N
P	NC	NC	Q8	SA	SA	C	SA	SA	NC	D0	Q0	P
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI	R

Pin Descriptions

Symbol	Type	Description	Notes
$\overline{BW0} - \overline{BW3}$	Input	Byte write controls	Sampled on rising edges of K clocks
C / $\overline{C}$	Input	Output clocks (active high/low)	
CQ / $\overline{CQ}$	Output	Output echo clock (active high/low)	
DN	Input	Synchronous data input	Sampled on rising edges of K clocks
$\overline{Doff}$	Input	Disable DLL (when low)	
K / $\overline{K}$	Input	Input clocks (active high/low)	
NC	---	Not connected to die or any other pin	
QN	Output	Synchronous data output	
$\overline{R}$	Input	Synchronous read port select	Sampled on rising edge of K
SA	Input	Synchronous address inputs	Sampled on rising edges of K clocks
TCK	Input	Test clock	For JTAG
TDI	Input	Test data input	For JTAG
TDO	Output	Test data output	For JTAG
TMS	Input	Test mode select	For JTAG
$\overline{W}$	Input	Synchronous write port select	Sampled on rising edge of K
VDD	Supply	Power supply; 1.8 V nominal	
VDDQ	Supply	Isolated output buffer supply	1.5 or 1.8 V nominal
VREF	Input	HSTL input reference voltage	
VSS	Supply	Ground	
ZQ	Input	Output impedance matching input	May be connected to VDDQ for minimum impedance
144 M	--	Available for expansion to 144 Mb	
288 M	--	Available for expansion to 288 Mb	

Functional Details

Clocks

K and $\overline{K}$ are the input clocks. The rising edges are used to capture all synchronous inputs and, in single-clock mode, to drive out data. All accesses are driven on the rising edge of K.

C and $\overline{C}$ are the optional output clocks. They can be used to deskew the flight times of various devices back to the controller by delaying data output as much as a few nanoseconds beyond the next rising edges of the K and $\overline{K}$ clocks. If C and $\overline{C}$ are tied high at power-on, the device operates in single-clock mode and the K clocks drive the outputs.

CQ and $\overline{CQ}$ are echo clocks that can be used to simplify data capture in high-speed systems. These clocks are normally referenced with respect to the C clocks; in single-clock mode, they are referenced with respect to the K clocks.

Burst Operations

Read and Write operations are synchronous pipelined "burst" operations. In every case where a read or write command is accepted by the RAM, it responds by issuing or accepting two beats of data in one clock cycle, executing data transfers on subsequent rising clock edges, as illustrated in the timing diagrams. It is not possible to stop a burst once it starts; two beats of data are always transferred.

Read and Write Ports

Data flows into the RAM though a dedicated Read port and out through a dedicated Write port. Each port has its own dedicated registers. Read and Write operations can be conducted concurrently. Address pins are multiplexed, with Read address sampled on the rising edge of K and Write address on the rising edge of $\overline{K}$.

Concurrent Transactions

The Read and Write ports are completely independent, and their addresses are latched on different clock edges, so the user can access any location on either port regardless of the status of the other port. Reads and Writes can also be started in the same clock cycle. When both ports initiate access to the same address in the same cycle, the Read is assumed to occur before the Write. The Read returns the most recent data associated the address, and may forward data from a Write that was initiated on the previous rising edge of K.

Read Operation

A Read is initiated by asserting $\overline{R}$ at the rising edge of K. The address is latched at that time and stored in the Read address register. After the next rising edge of K, the first word of data is driven out onto the Q pins using $\overline{C}$ as the timing reference and the second word of data is driven on the following rise of C. (In single clock mode, the K clocks are used in place of the C clocks.) The Q pins are automatically tri-stated following the next rising edge of the C clocks; this allows seamless transitions without wait states between devices in a depth expanded memory.

Write Operation

A Write is initiated by asserting $\overline{W}$ at the rising edge of K. At that time, the data on the D pins is latched into the lower half of the Write Data Register, subject to the values on the $\overline{BWn}$ pins (see below). On the subsequent rising edge of $\overline{K}$, the Write address is latched. At the same time, the data on the D pins is latched into the upper half of the Write Data Register, again subject to the values on the $\overline{BWn}$ pins. The data from the Write Data Register is then written into the specified address.

Byte Writes

During Write operations, the $\overline{BWn}$ pins are sampled at the same time as the D pins. The values on the $\overline{BWn}$ pins control the use of each byte of data. If a Byte Write pin is active (low), the corresponding byte of data is written; if inactive (high), the corresponding byte is ignored.

Example: x18 Write Sequence Using Byte Write Enables

Data In Sample Time	$\overline{BW0}$	$\overline{BW1}$	**D0–D8**	**D9–D17**
Beat 1	low	high	Data In	ignored
Beat 2	high	low	ignored	Data In

Resulting Write Operation:

Byte 1 D0–D8	**Byte 2 D9–D17**	**Byte 3 D0–D8**	**Byte 4 D9–D17**
Written	Unchanged	Unchanged	Written
Beat 1		Beat 2	

Byte Write Truth Tables

$\overline{BW}$ pins are always sampled on the same clock edge as the D pins.
H = high, L = low, X = don't care.

x36

$\overline{BW0}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	D0 – D8	D9 – D17	D18 – D26	D27 – D35
H	H	H	H	X	X	X	X
L	H	H	H	Data	X	X	X
H	L	H	H	X	Data	X	X
L	L	H	H	Data	Data	X	X
H	H	L	H	X	X	Data	X
L	H	L	H	Data	X	Data	X
H	L	L	H	X	Data	Data	X
L	L	L	H	Data	Data	Data	X
H	H	H	L	X	X	X	Data
L	H	H	L	Data	X	X	Data
H	L	H	L	X	Data	X	Data
L	L	H	L	Data	Data	X	Data
H	H	L	L	X	X	Data	Data
L	H	L	L	Data	X	Data	Data
H	L	L	L	X	Data	Data	Data
L	L	L	L	Data	Data	Data	Data

x18

$\overline{BW0}$	$\overline{BW1}$	D0 – D8	D9 – D17
H	H	X	X
L	H	Data	X
H	L	X	Data
L	L	Data	Data

Deselect

Either port is deselected when its Select pin ($\overline{W}$ or $\overline{R}$) is inactive (high) at the rising edge of K. All pending operations are completed, but other inputs are ignored. Deselecting one port does not affect the other, but both ports may be deselected at once by making both $\overline{W}$ and $\overline{R}$ inactive.

Truth Table

Operation	Clock Edge	$\overline{R}$	$\overline{W}$	SA	Data
Write	↑K	X	L	X	D (Write Address)
	↑$\overline{K}$	X	X	Write Address	D (Write Address + 1)
Read	↑K	L	X	Read Address	X
	↑$\overline{K}$	X	X	X	X
	↑C if double-clock, ↑K if single-clock	X	X	X	X
	↑$\overline{C}$ if double-clock, ↑$\overline{K}$ if single-clock	X	X	X	Q (Read Address)
	↑C if double-clock, ↑K if single-clock	X	X	X	Q (Read Address + 1)
NOP (Deselect)	↑K	H	H	X	Pending transactions finish, then D = X, Q = High-Z
Standby	Stopped	X	X	X	D and Q = Previous State

Notes: X = don't care; H = logic high; L = logic low; ↑ represents rising edge.

Programmable Impedance

An optional programmable impedance output driver can periodically adjust the impedance to compensate for drifts in supply voltage and temperature.

To enable this feature, connect the ZQ pin to Vss via an external resistor, RQ, with a value 5x the desired output impedance. The allowable range of RQ is between 175Ω and 350Ω with VDDQ = 1.5V. An internal calibration sequence occurs every 1024 cycles, and an update is performed during the next available deselected memory cycle. Each update may move the impedance level one step toward the optimum level.

To disable this feature, tie the ZQ pin directly to VDDQ. The device then runs with a constant minimum impedance.

DLL (Delay Lock Loop)

This device's DLL is designed to function between 80 MHz and the specified maximum clock frequency. The DLL may be disabled by applying ground to the $\overline{\text{Doff}}$ pin.

If the DLL is to be used, it is recommended that $\overline{\text{Doff}}$ be pulled high with a pullup resistor of 1 Kohm. At power-up or reset the DLL locks to the K clock. During operation, it can synchronize to either the K or C clock, so both clocks must have low phase jitter (see t_{KCVar} on page 13). During power-up, the DLL locks within 1024 cycles of stable clock after $\overline{\text{Doff}}$ is brought high. After power-up, the DLL can be reset either by taking $\overline{\text{Doff}}$ low for 30 ns and then bringing it high, or else by preventing a rising K clock edge for a minimum of 30 ns and then providing stable clock for 1024 cycles. If the DLL loses its lock during operation, a reset is not necessary; it will re-lock automatically within 1024 clock cycles after a stable clock is presented.

Note: If K is not stable when the DLL is enabled, the DLL may lock on the wrong frequency and cause undefined errors or failures during the initial stage.

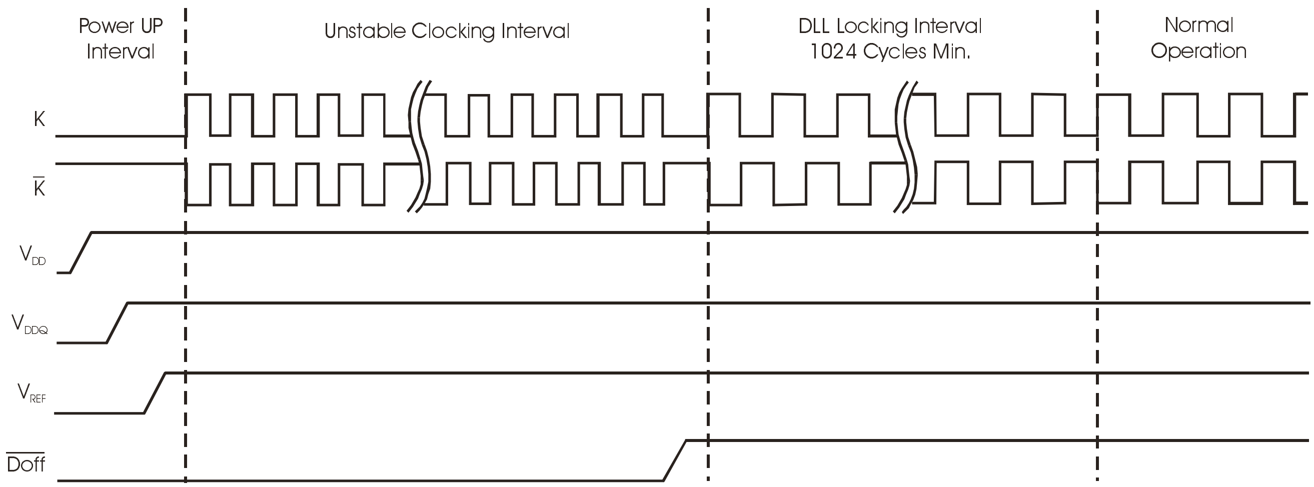
Power-Up Sequence

To prevent undefined operations, power up the device in this sequence:

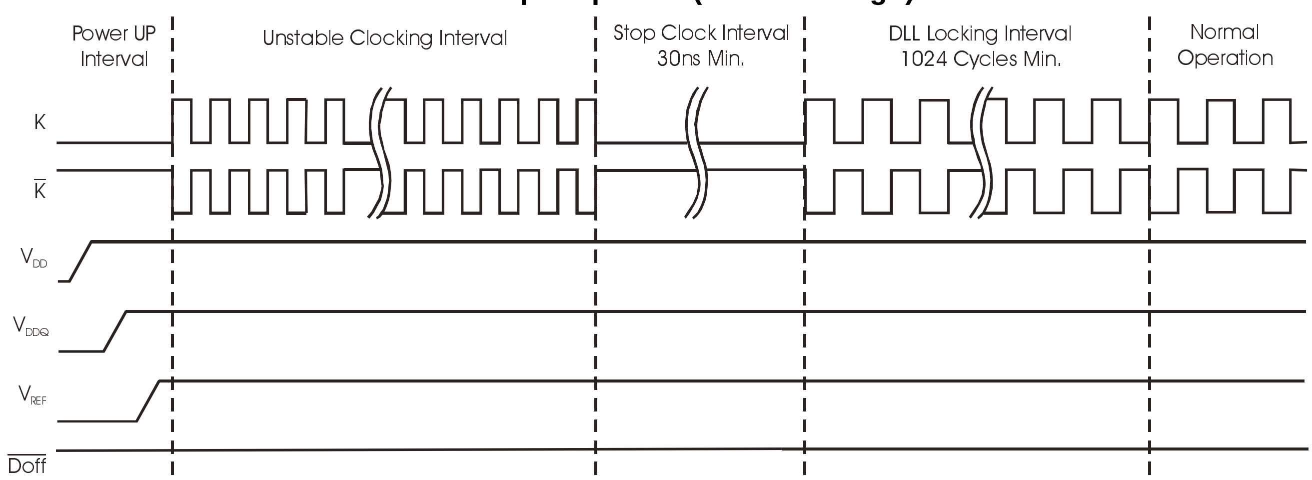
1. Apply power and hold $\overline{\text{Doff}}$ low (all other inputs are “don’t care”).
2. Apply VDD before VDDQ.
3. Apply VDDQ before VREF, or at the same time as VREF.
4. If using DLL: Allow power and clocks to stabilize, then take $\overline{\text{Doff}}$ high and wait 1024 clocks to ensure a lock. (If DLL is enabled while clocks are unstable it may lock to the wrong frequency, causing unstable RAM behavior.)

Note: $\overline{\text{Doff}}$ may be tied high. In this case, DLL should be reset (after the clocks become stable) by preventing a rising clock edge for at least 30 ns.

Power-Up Sequence ($\overline{\text{Doff}}$ Controlled)



Power-Up Sequence ($\overline{\text{Doff}}$ Tied High)



Maximum Ratings

Description	Value	Unit
Supply voltage on V_{DD} pins relative to Vss	-0.5 to 2.9	V
Supply voltage on V_{DDQ} pins relative to Vss	-0.5 to V_{DD}	V
DC output voltage in High-Z state	–0.5 to V_{DDQ} +0.5	V
DC input voltage (subject to overshoot/undershoot, see below)	–0.5 to V_{DD} +0.5	V
Static discharge voltage (per MIL-STD-883, method 3015)	> 2001	V
Output current (low)	20	mA
Latch-up current	>200	mA
Storage temperature	-65 to 150	°C
Ambient temperature (power applied)	-55 to +125	°C
Operating temperature (V_{DD} 1.8V ±0.1V and V_{DDQ} 1.4V to V_{DD}, assuming linear ramp at power-up within 200 ms, with V_{IH} < V_{DD} and V_{DDQ} • V_{DD}.)	0 to 70	°C
Overshoot: V_{IH}(AC) < V_{DDQ} + 0.85V, pulse width < tKHKH/2 Undershoot: V_{IL}(AC)> -1.5V, pulse width < tKHKH/2		

Note: Permanent damage to the device may occur if the Maximum Ratings are exceeded.

Electrical Characteristics

Over the operating range (0°C to 70°C), all voltages referenced to Ground

DC Voltage

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		1.7	1.8	1.9	V
V_{DDQ}	I/O Supply voltage		1.4	1.5	V_{DD}	V
V_{OH}	Output high voltage	Impedance controlled, I_{OH} = -(V_{DDQ}/2)/(RQ/5), 175• <= RQ <= 350•	V_{DDQ}/2 – 0.12		V_{DDQ}/2 + 0.12	V
		Nominal impedance, I_{OH} = –0.1 mA	V_{DDQ} – 0.2		V_{DDQ}	V
V_{OL}	Output low voltage	Impedance controlled, I_{OL} = (V_{DDQ}/2)/(RQ/5), 175• <= RQ <= 350•	V_{DDQ}/2 – 0.12		V_{DDQ}/2 + 0.12	V
		Nominal impedance, I_{OL} = 0.1 mA	Vss		0.2	V
V_{IH}	Input high voltage	Overshoot: V_{IH}(AC) < V_{DDQ} + 0.85V, pulse width < tKHKH /2 Undershoot: V_{IL}(AC)> -1.5V, pulse width < tKHKH /2	V_{REF} + 0.1		V_{DDQ} + 0.3	V
V_{IL}	Input low voltage		– 0.3		V_{REF} – 0.1	V
V_{REF}	Reference voltage		Greater of: 0.68 or 0.46 * V_{DDQ}	0.75	Lesser of: 0.95 or 0.54 * V_{DDQ}	V

DC Current

Parameter	Description	Test Conditions	Speed	Min	Max	Unit
I_X	Input leakage current	Ground <= V_I <= V_{DDQ}		–5	5	•A
I_{OZ}	Output leakage current	Ground <= V_I <= V_{DDQ}, output disabled		–5	5	•A
I_{DD}	V_{DD} operating supply	V_{DD} = max, I_{OUT} = 0 mA, f = f_{MAX} = 1/ tKHKH	333 MHz	tbd	tbd	mA
			300 MHz	tbd	tbd	mA
			267 MHz	tbd	tbd	mA
			250 MHz	tbd	tbd	mA
			200 MHz	tbd	tbd	mA
			167 MHz	tbd	tbd	mA
I_{SB1}	Automatic power-down current	Both ports deselected, Inputs static, V_{DD} = max, V_{IN} >= V_{IH} or V_{IN} <= V_{IL}, f = f_{MAX} = 1/ tKHKH	333 MHz	tbd	tbd	mA
			300 MHz	tbd	tbd	mA
			267 MHz	tbd	tbd	mA
			250 MHz	tbd	tbd	mA
			200 MHz	tbd	tbd	mA
			167 MHz	tbd	tbd	mA

AC Input Requirements

Parameter	Description	Min	Max	Unit
V_{IH}	Input high voltage	V_{REF} + 0.2	--	V
V_{IL}	Input low voltage	--	V_{REF} – 0.2	V

Capacitance

Tested initially, and after any design or process change that might affect these parameters

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25°C, f = 1MHz, V_{DD} = 1.8V, V_{DDQ} = 1.5 V	5.5	pF
C_{CLK}	Clock input capacitance		8.5	pF
C_O	Output capacitance		8.0	pF

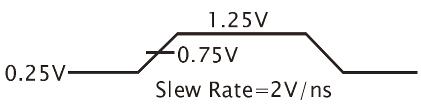
Thermal Resistance

Tested initially, and after any design or process change that might affect these parameters

Parameter	Description	Test Conditions	FBGA	Unit
•ja	Junction to Ambient	Standard methods and procedures per EIA/JESD51	16.2	°C/W
•jc	Junction to Case		2.3	°C/W

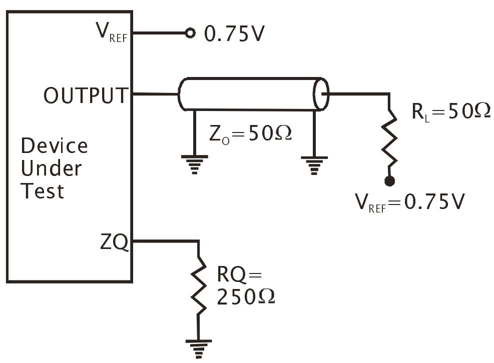
AC Waveform

(All input pulses)



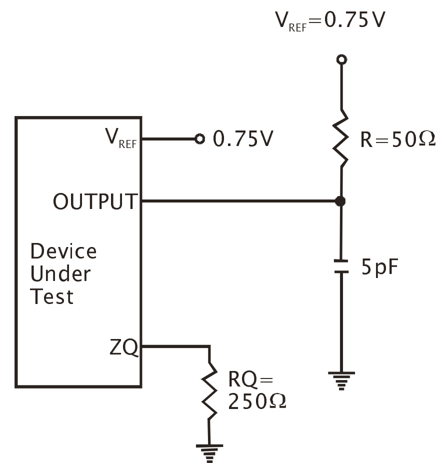
AC Test Loads

VDDQ = 1.5V



TEST CONFIGURATION “A”

Applies to all measurements unless specified otherwise.



TEST CONFIGURATION “B”

Applies only to the measurement of tCHZ and tCLZ.

Switching Characteristics

All measurements in ns unless specified otherwise

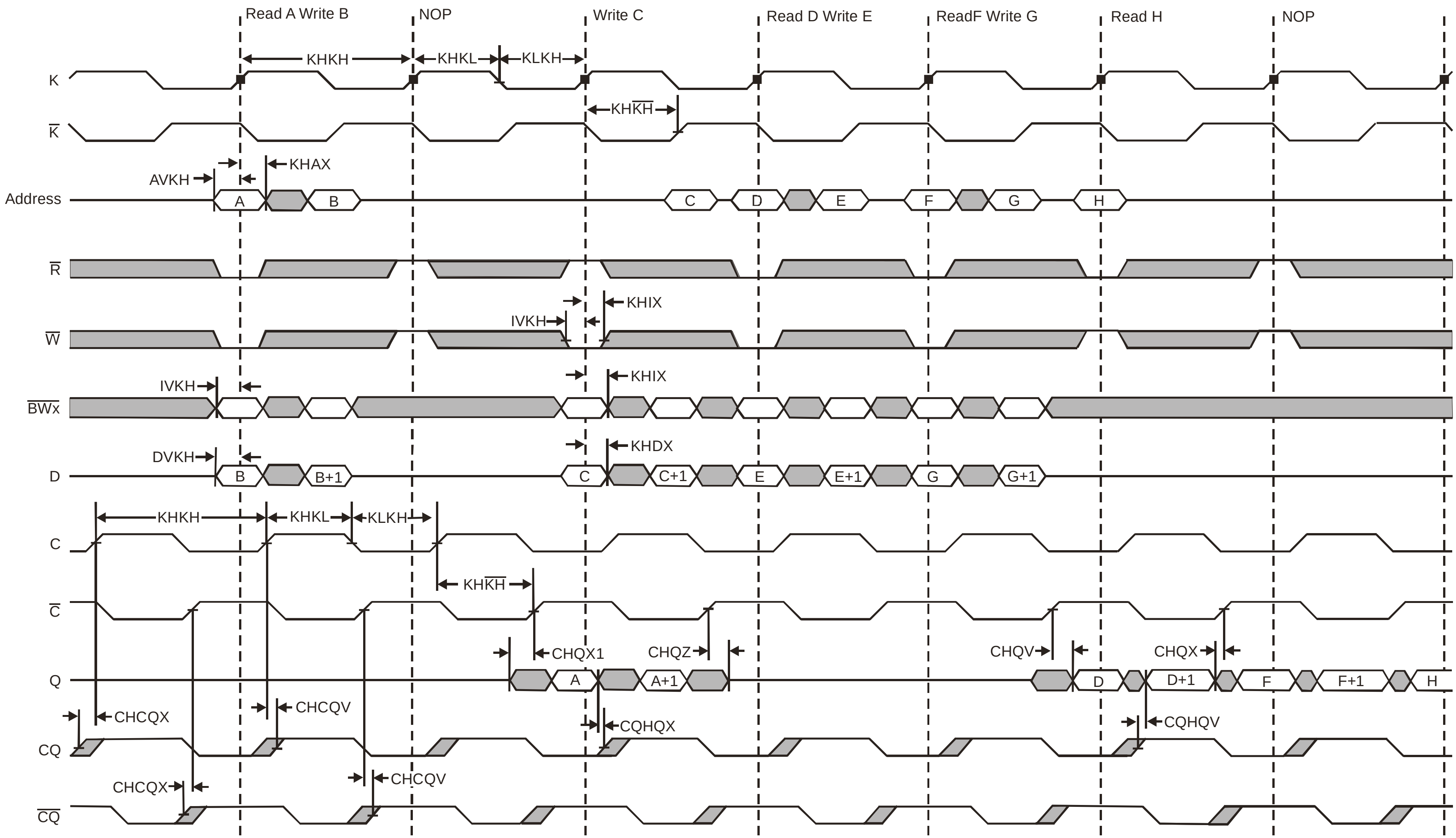
Parameter	Symbol	333 MHz		300 MHz		267 MHz		250 MHz		200 MHz		167 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
V_{DD} valid to first read/write access	tPOWER	minimum: 1 ms											
Clock Timing													
K / $\overline{K}$ / C / $\overline{C}$ clock cycle time	tKHKH	tbd	tbd	tbd	tbd	tbd	tbd	4.0	6.3	5.0	7.9	6.0	8.4
K / $\overline{K}$ / C / $\overline{C}$ clock high pulse width	tKHKL	tbd	--	tbd	--	tbd	--	1.6	--	2.0	--	2.4	--
K / $\overline{K}$ / C / $\overline{C}$ clock low pulse width	tKLKH	tbd	--	tbd	--	tbd	--	1.6	--	2.0	--	2.4	--
K rise to $\overline{K}$ rise, C rise to $\overline{C}$ rise	tKH$\overline{KH}$	tbd	--	tbd	--	tbd	--	1.8	--	2.2	--	2.7	--
K rise to C rise, $\overline{K}$ rise to $\overline{C}$ rise	tKHCH	0.0	tbd	0.0	tbd	0.0	tbd	0.0	1.8	0.0	2.2	0.0	2.7
Output Timing													
C / $\overline{C}$ (or K / $\overline{K}$) rise to data valid	tCHQV	--	tbd	--	tbd	--	tbd	--	0.45	--	0.45	--	0.50
C / $\overline{C}$ (or K / $\overline{K}$) rise to data hold	tCHQX	tbd	--	tbd	--	tbd	--	-0.45	--	-0.45	--	-0.50	--
C / $\overline{C}$ (or K / $\overline{K}$) rise to echo clock valid	tCHCQV	--	tbd	--	tbd	--	tbd	--	0.45	--	0.45	--	0.50
C / $\overline{C}$ (or K / $\overline{K}$) rise to echo clock hold	tCHCQX	tbd	--	tbd	--	tbd	--	-0.45	--	-0.45	--	-0.50	--
CQ, $\overline{CQ}$ rise to data valid	tCQHQV	--	tbd	--	tbd	--	tbd	--	0.30	--	0.35	--	0.40
CQ, $\overline{CQ}$ rise to data hold	tCQHQX	tbd	--	tbd	--	tbd	--	-0.30	--	-0.35	--	-0.40	--
C / $\overline{C}$ (or K / $\overline{K}$) rise to High-Z [note 3]	tCHQZ	--	tbd	--	tbd	--	tbd	--	0.45	--	0.45	--	0.50
C / $\overline{C}$ (or K / $\overline{K}$) rise to Low-Z [note 3]	tCHQX1	tbd	--	tbd	--	tbd	--	-0.45	--	-0.45	--	-0.50	--
Setup Timing													
Address setup to K rise	tAVKH	tbd	--	tbd	--	tbd	--	0.35	--	0.40	--	0.50	--
$\overline{R}$ / $\overline{W}$ / $\overline{BWn}$ setup to K / $\overline{K}$ rise	tIVKH	tbd	--	tbd	--	tbd	--	0.35	--	0.40	--	0.50	--
Dn setup to K / $\overline{K}$ rise	tDVKH	tbd	--	tbd	--	tbd	--	0.35	--	0.40	--	0.50	--
Hold Timing													
Address hold after K rise	tKHAX	tbd	--	tbd	--	tbd	--	0.35	--	0.40	--	0.50	--
$\overline{R}$ / $\overline{W}$ / $\overline{BWn}$ hold after K / $\overline{K}$ rise	tKHIX	tbd	--	tbd	--	tbd	--	0.35	--	0.40	--	0.50	--
Dn hold after K / $\overline{K}$ rise	tKHDX	tbd	--	tbd	--	tbd	--	0.35	--	0.40	--	0.50	--
DLL Timing													
Clock phase jitter	tKCVar	--	0.20	--	0.20	--	0.20	--	0.20	--	0.20	--	0.20
DLL lock time (K or C)	tKCLock	minimum: 1024 clock cycles											
K static to DLL reset	tKCReset	30	--	30	--	30	--	30	--	30	--	30	--

Notes:

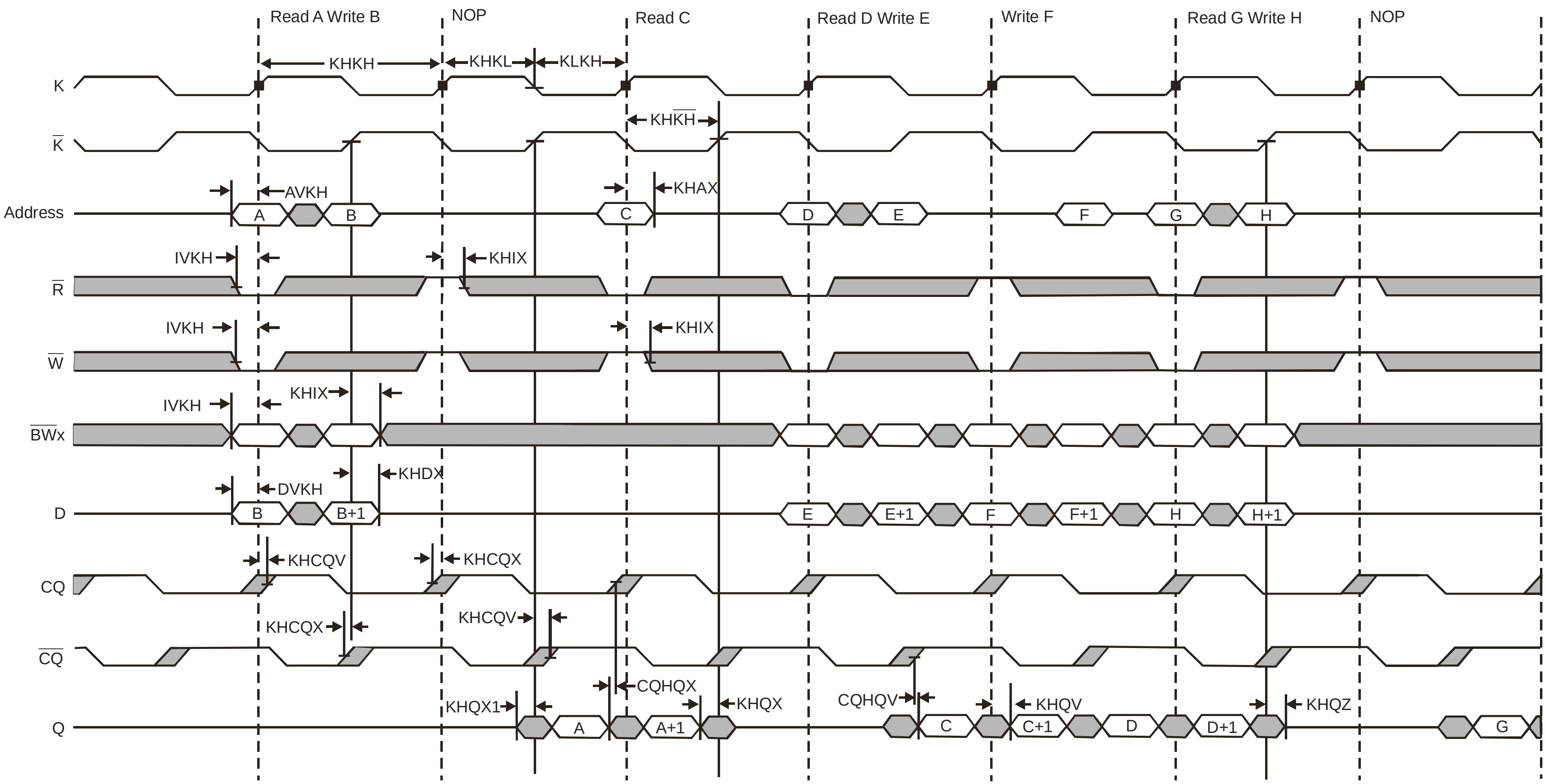
1. All measurements are over the operating range (0°C to 70°C)
2. Any part may be operated at a frequency lower than its defined speed rating. In this case, the part requires the input timings of that frequency, and will output data with the output timings of that frequency.
3. tCHQZ and tCHQX1 use test configuration “B” (see page 12). Transition is measured ±100 mV from steady-state voltage. tCHQZ is always less than tCHQX1, and tCHQX1 is always less than tCHQV.

Timing Diagrams

C/$\overline{C}$ Controlled Write, K/$\overline{K}$ Controlled Read



K/$\overline{K}$ Controlled Write and Read



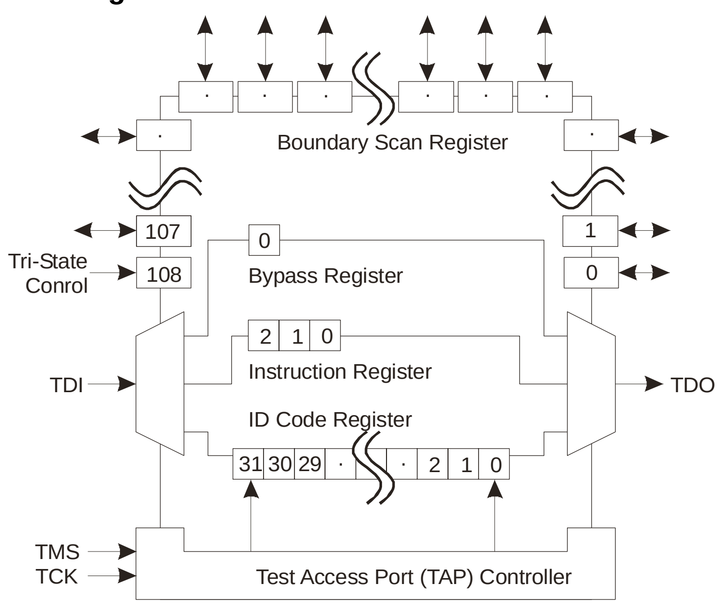
JTAG Port Operation

Overview

This device incorporates a serial boundary scan interface that complies with IEEE Standard 1149.1-1990, commonly known as JTAG. The JTAG Port is also known as a Test Access Port, or TAP. It can be used to read the device ID code, monitor all RAM input and I/O pads, drive pre-loaded values into the I/O bus, or the I/O bus to a High-Z state.

The port's input interface levels scale with V_{DD} and the output drivers are powered by V_{DDQ}. The port is reset at power-up and remains inactive until clocked. Pins, registers, states, and instructions are described below.

JTAG Test Access Port Block Diagram



JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all events. Inputs are captured on the rising edge; outputs are driven on the falling edge.
TMS	Test Mode Select	In	Command input for the JTAG state machine, sampled on the rising edge of TCK.
TDI	Test Data In	In	The input side of any selected register, sampled on the rising edge of TCK.
TDO	Test Data Out	Out	The output side of any selected register, driven on the falling edge of TCK.

Notes: TCK, TDI, and TMS have internal pull-up circuits; when undriven they produce a logic one input level.

This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The JTAG controller is reset automatically at power-up, and again whenever it enters the Test-Logic-Reset state.

The "selected" register is determined by the current instruction and the state of the JTAG controller.

Disabling the JTAG Port

For normal operation of the device without using JTAG, the controller can be held in a permanent Reset state. To do this, TCK, TDI, and TMS are left floating or tied to either V_{DD} or V_{SS}. TDO should be left unconnected.

JTAG Registers

The JTAG interface has four serial shift registers that are used in conjunction with JTAG instructions. When a register is selected, it is placed between TDI and TDO so that it can shift data out serially on the falling edges of TCK and capture input data on the rising edges of TCK, depending on the state of the controller.

Instruction Register

The three-bit Instruction Register holds an instruction to be executed. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller enters the Test-Logic-Reset state. The user may load instructions through the TDI pin using the various IR (Instruction Register) states. The Instruction Register is always selected in the IR states, regardless of the current instruction.

Bypass Register

The single-bit Bypass Register can be placed between TDI and TDO to pass serial data through the JTAG Port with as little delay as possible. The Bypass Register is selected by the BYPASS instruction.

Identification (ID) Register

The 32-bit ID Register receives an identification code from an on-chip ID ROM. The code describes various attributes of the RAM as indicated in the table below. The ID Register is selected by the IDCODE instruction.

ID Code Contents

	Die Revision Code				Not Used								I/O Configuration								Tezzaron Semiconductor JEDEC Vendor ID Code											Presence Register
Bit#	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
x9	X	X	X	X	0	0	0	0	0	0	0	0	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	0	0	0	0	0	1	0	1	1	0	0	1
x18	X	X	X	X	0	0	0	0	0	0	0	0	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	0	0	0	0	0	1	0	1	1	0	0	1
x36	X	X	X	X	0	0	0	0	0	0	0	0	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	0	0	0	0	0	1	0	1	1	0	0	1

Boundary Scan Register

The Boundary Scan Register is a chain of 109 cells. Each cell contains a Scan bit and an Update bit. The Scan bits can capture the logic level found on the RAM's I/O pins; the Update bits can drive a preloaded set of data onto the RAM's outputs. The Boundary Scan Register cells are daisy chained together so their contents can be shifted out serially through the TDO pin and loaded through the TDI pin. The relationship between the device pins and the cells in the Boundary Scan Register is described in the Scan Order Table below; note that the register includes a number of special purpose cells that do not represent I/O pins. The Boundary Scan Register is selected by the SAMPLE-Z, SAMPLE/PRELOAD, and EXTEST instructions.

Scan Order Table

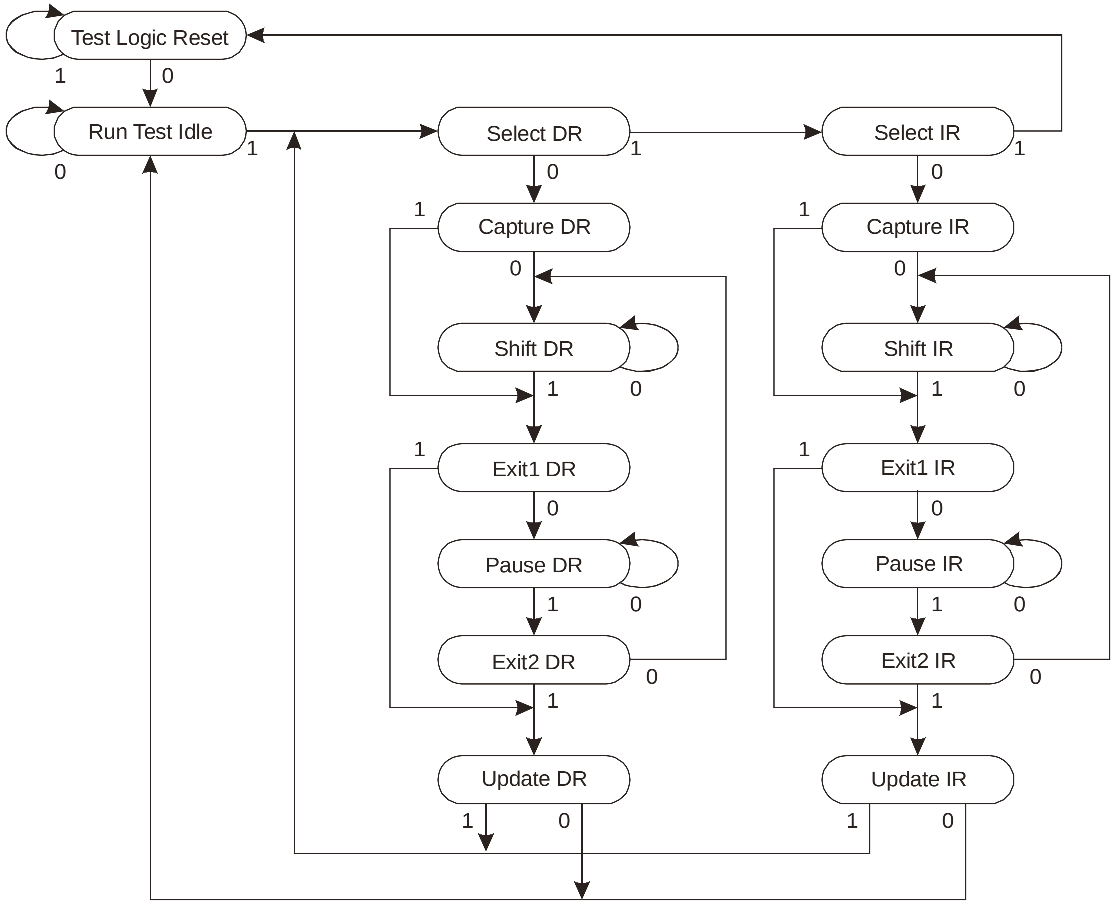
Cell#	Pin Name	I/O	Notes
0	tbd	tbd	
1	tbd	tbd	
2	tbd	tbd	
3	tbd	tbd	
4	tbd	tbd	
5	tbd	tbd	
6	tbd	tbd	
7	tbd	tbd	
8	tbd	tbd	
9	tbd	tbd	
10	tbd	tbd	
11	tbd	tbd	
12	tbd	tbd	
13	tbd	tbd	
14	tbd	tbd	
15	tbd	tbd	
16	tbd	tbd	
17	tbd	tbd	
18	tbd	tbd	
19	tbd	tbd	
20	tbd	tbd	
21	tbd	tbd	
22	tbd	tbd	
23	tbd	tbd	
24	tbd	tbd	
25	tbd	tbd	
26	tbd	tbd	
27	tbd	tbd	

Cell#	Pin Name	I/O	Notes
28	tbd	tbd	
29	tbd	tbd	
30	tbd	tbd	
31	tbd	tbd	
32	tbd	tbd	
33	tbd	tbd	
34	tbd	tbd	
35	tbd	tbd	
36	tbd	tbd	
37	tbd	tbd	
38	tbd	tbd	
39	tbd	tbd	
40	tbd	tbd	
41	tbd	tbd	
42	tbd	tbd	
43	tbd	tbd	
44	tbd	tbd	
45	tbd	tbd	
46	tbd	tbd	
47	tbd	tbd	
48	tbd	tbd	
49	tbd	tbd	
50	tbd	tbd	
51	tbd	tbd	
52	tbd	tbd	
53	tbd	tbd	
54	tbd	tbd	
55	tbd	tbd	

Cell#	Pin Name	I/O	Notes
56	tbd	tbd	
57	tbd	tbd	
58	tbd	tbd	
59	tbd	tbd	
60	tbd	tbd	
61	tbd	tbd	
62	tbd	tbd	
63	tbd	tbd	
64	tbd	tbd	
65	tbd	tbd	
66	tbd	tbd	
67	tbd	tbd	
68	tbd	tbd	
69	tbd	tbd	
70	tbd	tbd	
71	tbd	tbd	
72	tbd	tbd	
73	tbd	tbd	
74	tbd	tbd	
75	tbd	tbd	
76	tbd	tbd	
77	tbd	tbd	
78	tbd	tbd	
79	tbd	tbd	
80	tbd	tbd	
81	tbd	tbd	
82	tbd	tbd	
83	tbd	tbd	

Cell#	Pin Name	I/O	Notes
84	tbd	tbd	
85	tbd	tbd	
86	tbd	tbd	
87	tbd	tbd	
88	tbd	tbd	
89	tbd	tbd	
90	tbd	tbd	
91	tbd	tbd	
92	tbd	tbd	
93	tbd	tbd	
94	tbd	tbd	
95	tbd	tbd	
96	tbd	tbd	
97	tbd	tbd	
98	tbd	tbd	
99	tbd	tbd	
100	tbd	tbd	
101	tbd	tbd	
102	tbd	tbd	
103	tbd	tbd	
104	tbd	tbd	
105	tbd	tbd	
106	tbd	tbd	
107	tbd	tbd	
108	Tri-State Control	n/a	

JTAG Controller State Diagram



JTAG Controller States

Overview

The JTAG controller is inactive until clocked with TCK. When TCK is activated, the controller is in the Test Logic Reset state. Subsequent transitions between states are controlled by the TMS signal as shown in the diagram above. TMS is sampled at each rising edge of TCK.

The DR states select and manipulate the four JTAG data registers; the IR states select and manipulate the Instruction Register.

Test Logic Reset

In this state, the IDCODE instruction is loaded into the Instruction Register, no control is exerted over the RAM's output pins, and the RAM executes as if the JTAG port were disabled. If TMS is held at 1 for five cycles, the controller returns to this state and loops until it detects a TMS value of 0.

Run Test Idle

This is the entry point for all instructions. The controller can loop here as needed, but performs no functions.

Select DR

The controller selects a data register (determined by the current instruction) and places it between TDI and TDO.

Capture DR

Depending upon the current instruction, the selected register may receive data from sources other than TDI.

Shift DR

On the falling edge of TCK, the least significant bit of the selected register is shifted onto TDO. On the rising edge of TCK, the value on the TDI pin is captured and shifted into the most significant bit of the selected register.

Exit1 DR

Data movement stops. No function is performed.

Pause DR

The controller can loop here, but performs no functions.

Exit2 DR

No function is performed.

Update DR

If the current instruction is SAMPLE or EXTEST, data in the Boundary Scan Register is copied from the Scan bits to the Update bits. Otherwise, no function is performed.

Select IR

The Instruction Register is selected and placed between TDI and TDO.

Capture IR

The controller loads the two least significant bits of the Instruction Register with 01.

Shift IR, Exit1 IR, Pause IR, Exit2 IR

These states are analogous to Shift DR, Exit1 DR, Pause DR, and Exit2 DR.

Update IR

Instruction loading is complete; the instruction is decoded for implementation. If the new instruction is EXTEST or SAMPLE-Z, JTAG exerts control over the RAM's output pins; otherwise, it releases control of those pins.

JTAG Controller Instruction Set

Instruction Summary

Instruction	Binary Code	Description
EXTEST	000	Either drives contents onto RAM outputs or forces outputs to High-Z; selects Boundary Scan Register; captures I/O ring contents; allows reading/loading of Boundary Scan Register.
IDCODE	001	Selects and loads ID Register; allows reading of register. **Default instruction** – automatically loaded in test-logic-reset state.
SAMPLE-Z	010	Forces all RAM outputs to High-Z; selects Boundary Scan Register; captures I/O ring contents; allows reading of Boundary Scan Register.
RFU	011	Do not use this instruction; reserved for future use. (Currently replicates BYPASS instruction.)
SAMPLE/PRELOAD	100	Selects Boundary Scan Register; captures I/O ring contents; allows reading/loading of Boundary Scan Register.
TEZZARON	101	Tezzaron private instruction; do not use.
RFU	110	Do not use this instruction; Reserved for Future Use. (Currently replicates BYPASS instruction.)
BYPASS	111	Selects Bypass Register; allows rapid pass-through of data.

Instruction Descriptions

NOTE: Several of these instructions capture signals from the RAM's I/O ring. The user must be aware that the JTAG clock (TCK) operates at 20 MHz or less, while the RAM clock operates more than an order of magnitude faster. Because of the difference in clock frequencies, it is possible that an input or output will undergo a transition during the capture. In this case, the signal may be captured while in transition. This will not harm the device, but there is no guarantee as to the value that will be captured, and repeatable results may not be possible. To guarantee that the correct value of a signal is captured, the signal must be stabilized long enough to meet the JTAG set-up plus hold times (tTS + tTH). If there is no way in a design to stop (or slow) the RAM clock, the RAM clock inputs might not be captured correctly; however, it is still possible to capture all other signals and simply ignore the captured values of the RAM clock signals.

BYPASS

This instruction allows test data to pass through the device with minimal delay, to facilitate testing of other devices on the scan path.

Select-DR: The Bypass Register is placed between TDI and TDO.

Shift-DR: Data is shifted out through TDO and in from TDI.

SAMPLE/PRELOAD

This instruction allows sample data to be captured and examined without interfering with normal device operation. It also allows test data to be pre-loaded for later use with the EXTEST instruction.

Select-DR: The Boundary Scan Register is placed between TDI and TDO.

Capture-DR: A snapshot of data from all the RAM's I/O pins is captured in the Scan bits of the cells.

Shift-DR: Data in the Scan bits is shifted out serially through TDO and data presented to TDI is shifted in.

Update-DR: Data from the Scan bits is copied into the Update bits for later use (see EXTEST).

EXTEST

This instruction captures sample data and sets up test data, much like SAMPLE/PRELOAD, but it also controls the RAM's output pins. EXTEST is for testing only, as it will disrupt normal operation of the device. As soon as the EXTEST instruction is loaded (in Update-IR), it exerts control over the RAM's output pins and does not release them until a new instruction is loaded. The values in the Boundary Scan Register's Update bits are driven onto the output pins, *unless the Tri-State Control cell has been set (see below)*, in which case the output pins are tri-stated.

EXTEST and Tri-State

The Boundary Scan Register's last cell, #108, is the Tri-State Control cell. During EXTEST, it directly controls the state of the RAM's output pins. When HIGH, it enables the Update bit values to drive the output bus; when LOW, it places the output bus into a High-Z condition. The Tri-State Control cell's value is set to HIGH whenever the controller is in the "Test-Logic-Reset" state. The value is changed with the SAMPLE/PRELOAD or EXTEST instruction by shifting the desired value into the cell during the Shift-DR state. During Update-DR, the new value is copied into the cell's Update bit. From there, it controls the EXTEST instruction's behavior.

Select-DR: The Boundary Scan Register is placed between TDI and TDO.

Capture-DR: A snapshot of data from all the RAM's I/O pins is captured in the Scan bits of the cells.

Shift-DR: Data in the Scan bits is shifted out serially through TDO and data presented to TDI is shifted in.

Update-DR: Data in the Scan bits is copied to the Update bits. The values take effect immediately, driving the RAM's output bus as directed.

IDCODE

IDCODE is the default instruction, loaded automatically whenever the controller is placed in the Test-Logic-Reset state. It allows access to the device's internal ID ROM contents.

Select-DR: The ID Register is placed between TDI and TDO.

Capture-DR: The ID Register is loaded with the device's 32-bit identification code from the ID ROM.

Shift-DR: The contents of the ID Register is shifted out through TDO.

SAMPLE-Z

This instruction functions somewhat like EXTEST, except that the output bus is always tri-stated and the Update bits are not changed. Like EXTEST, it is disruptive to normal device operation. As soon as the SAMPLE-Z instruction is loaded (in Update-IR), it exerts control over the RAM's output pins and does not release them until a new instruction is loaded.

Select-DR: The Boundary Scan Register is connected between TDI and TDO.

Capture-DR: A snapshot of data from all the RAM's I/O pins is captured in the Scan bits.

Shift-DR: Data in the Scan bits is shifted out serially through TDO.

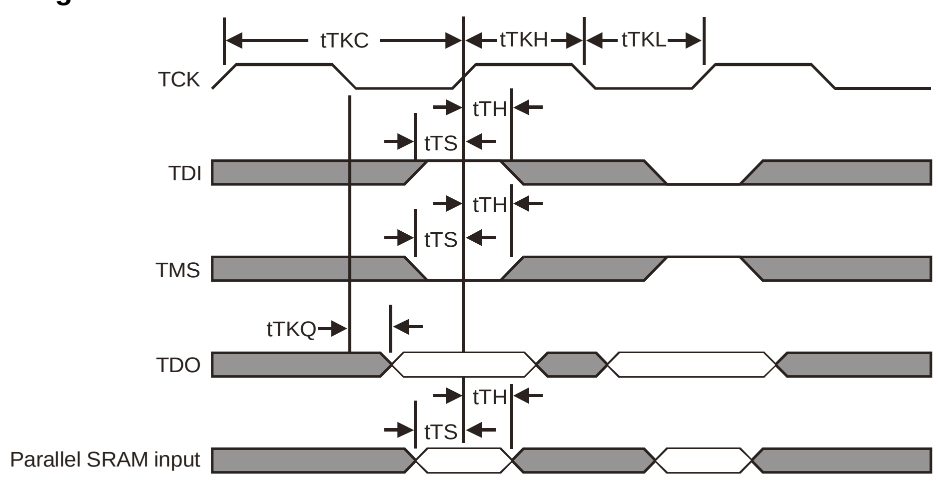
Tezzaron

This instruction is reserved for vendor use; do not use.

RFU

This instruction is reserved for future use; in this device it replicates the BYPASS instruction.

JTAG Port Timing Diagram



JTAG Port Recommended Operating Conditions and DC Characteristics (V)

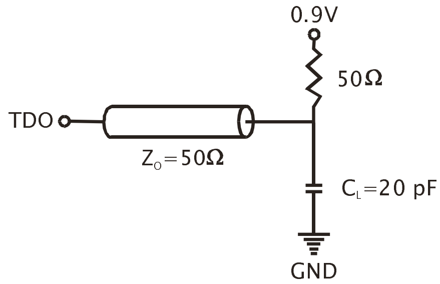
Parameter	Symbol	Min.	Typ.	Max.
Power Supply Voltage	V_{DDQ}	1.7	1.8	1.9
Input High Voltage	V_{IH}	1.3	--	V_{DD} + 0.3
Input Low Voltage	V_{IL}	–0.3	--	0.5
Output High Voltage (I_{OH} = -2 mA)	V_{OH}	1.4	--	V_{DD}
Output Low Voltage (I_{OL} = 2 mA)	V_{OL}	V_{SS}	--	0.4

Note: During JTAG operation, the input level of the RAM pins must conform to the device's DC specifications.

JTAG Port AC Test Conditions

Parameter	Symbol	Min	Unit
Input High/Low Level	V_{IH}/V_{IL}	1.3/0.5	V
Input Rise/Fall Time	TR/TF	1.0/1.0	ns
Input and Output Timing Reference Level	--	0.9	V

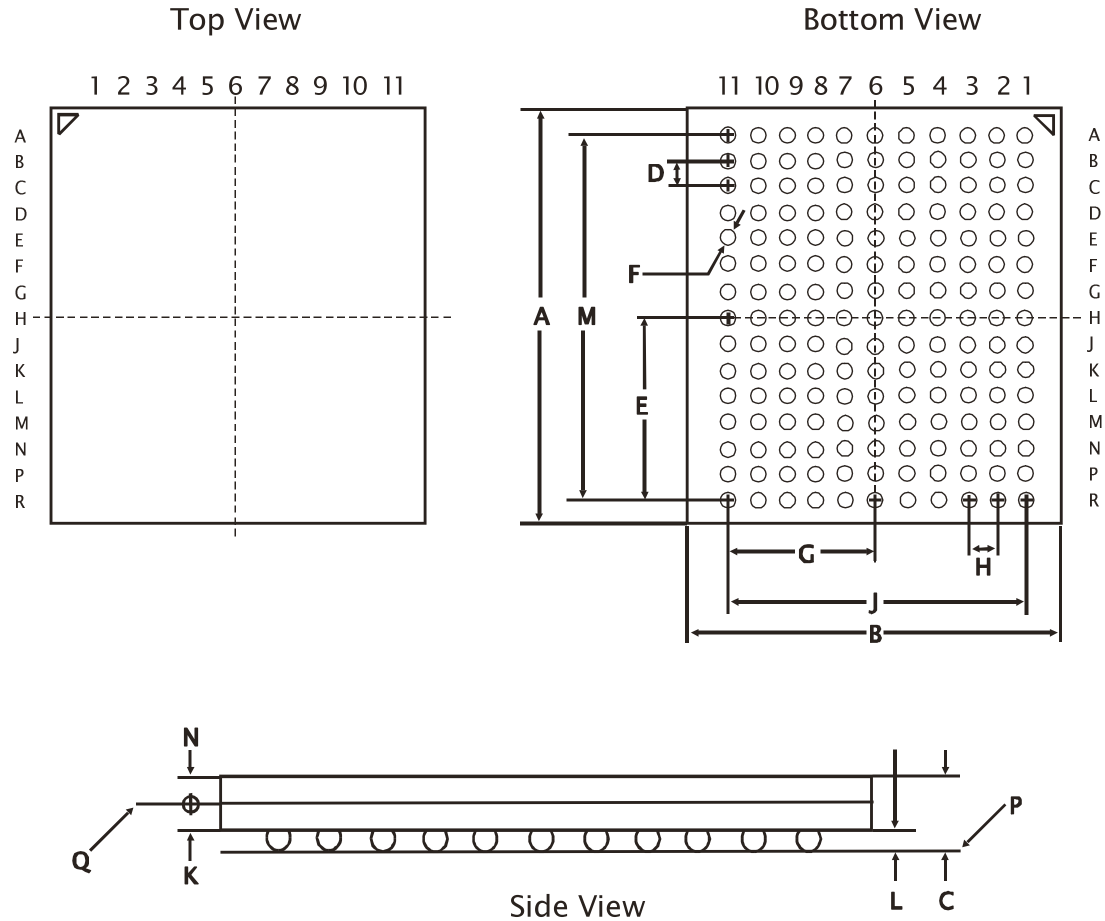
Parameters are measured with distributed scope and test jig capacitance.
Conditions as shown in diagram below unless otherwise noted.



JTAG Port AC Electrical Characteristics (ns)

Parameter	Symbol	Min	Max
TCK Cycle Time	tTKC	50	—
TCK High Pulse Width	tTKH	20	—
TCK Low Pulse Width	tTKL	20	—
Set Up Time – (TDI, TMS, Capture)	tTS	5	—
Hold Time – (TDI, TMS, Capture)	tTH	5	—
TCK Low to TDO Valid	tTKQ	0	10

Package Drawing



Symbol	Description	Measurement (mm)
A	Chip Length	17.00±0.10
B	Chip Width	15.00±0.10
C	Chip Height	1.40 max.
D	Length between pin centers	1.00
E	Length between center pin and outermost pin	7.00
F	Pin diameter	0.50 +0.14 / -0.06
G	Width between center pin and outermost pin	5.00
H	Width between pin centers	1.00
J	Width between outermost pins	10.00
K	Height of circuit card	0.36
L	Height of pins	0.35±0.06

Symbol	Description	Measurement (mm)
M	Length between outermost pins	14.00
N	Height of encapsulant	0.53±0.05
P	Seating Plane *	
Q	Top Plane of circuit card **	

Pin centers: within 0.05 mm of relative position at MMC
Pin centers: within 0.25 mm of true position at MMC
Package length/width edges: uniform within 0.15 mm
Package weight: tbd
Solder pad type NSMD (non-solder mask defined)
JEDEC reference: MO-216 – design 4.6C

* Seating plane surface uniform within 0.15 mm
** Top plane parallel to seating plane within 0.25 mm

Document History

Datasheet for TSC3Q272S09 / 18 / 36

Revision	Date	Changes
1.0	October 20, 2006	Original
1.1	23 January 2007	Added package letter, added QTRII trademark, corrected typos

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