

## FaStack® Stacking Technology

### Stacking Overview

This document examines the physical wafer-stacking process used to build Tezzaron's FaStack® multi-wafer stacks.

#### *Concept*

Electrical components are typically built into the surface layer of a silicon wafer, creating an essentially two-dimensional device. Stacking and interconnecting several silicon wafers enables the creation of truly three-dimensional devices.

#### *Benefits*

- **Density:** Integrating several layers of components into a stack multiplies the capacity of the finished chip without increasing its footprint.
- **Optimized Processing:** Gathering similar components onto specialized layers allows highly optimized wafer processing.
- **Heterogeneous Integration:** Incompatible processes may be run on separate wafers, then stacked into a single device.
- **Speed/Power:** Vertical stacking enables shorter physical connections for higher speed and lower power usage.

#### *Challenges*

- **Thermal buildup:** Thick stacks of silicon can trap heat, causing thermal stress.
- **Bonding:** Without excellent wafer-to-wafer bonds, yield will be unacceptably low.
- **Packaging:** Wafer stacks thicker than 400 microns cannot be accommodated in standard packaging.

### FaStack® Process Details

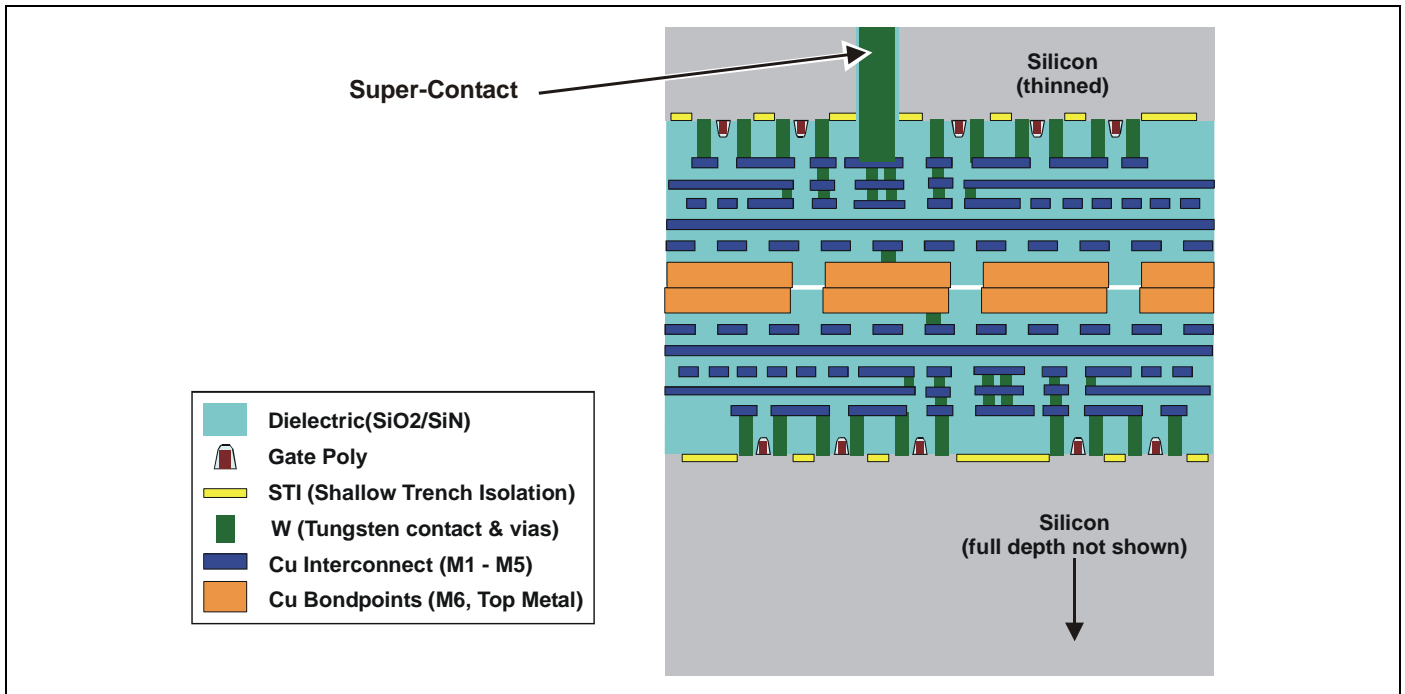
A semiconductor wafer is usually about 750 microns thick, but its electrical activity is confined to a surface layer from 4 to 10 microns thick. The functional part of a wafer is thus a tiny proportion of its thickness; the rest of the wafer contributes only structural support. The FaStack process uses most of the structural base of the first silicon wafer, but keeps less than 15 microns of each additional wafer in the stack. This produces multi-layer chips that fit easily into standard packaging.

Tezzaron's patented stacking process begins by building hundreds of thousands of vertical interconnect structures (Super-Contacts™) into the circuitry during normal wafer processing. The wafers are then metallized by coating them with a 0.5-micron SiO<sub>2</sub> insulating glass layer and then a 1.0-micron Cu metal bondpoint layer\* with a proprietary layout design. Using a thermal diffusion bonding process at less than 400°C, two metallized wafers are aligned with their front sides facing one another and then bonded together. Alignment and bonding are done using standard equipment available from EV Group (Austria), producing a metal-to-metal bond. The structural base (back side) of the upper wafer is then thinned to less than 10 microns by using a combination of conventional wafer grinding, spin-etching, and chemical-mechanical polishing. The thinning exposes the Super-Contacts that were built into the wafer.

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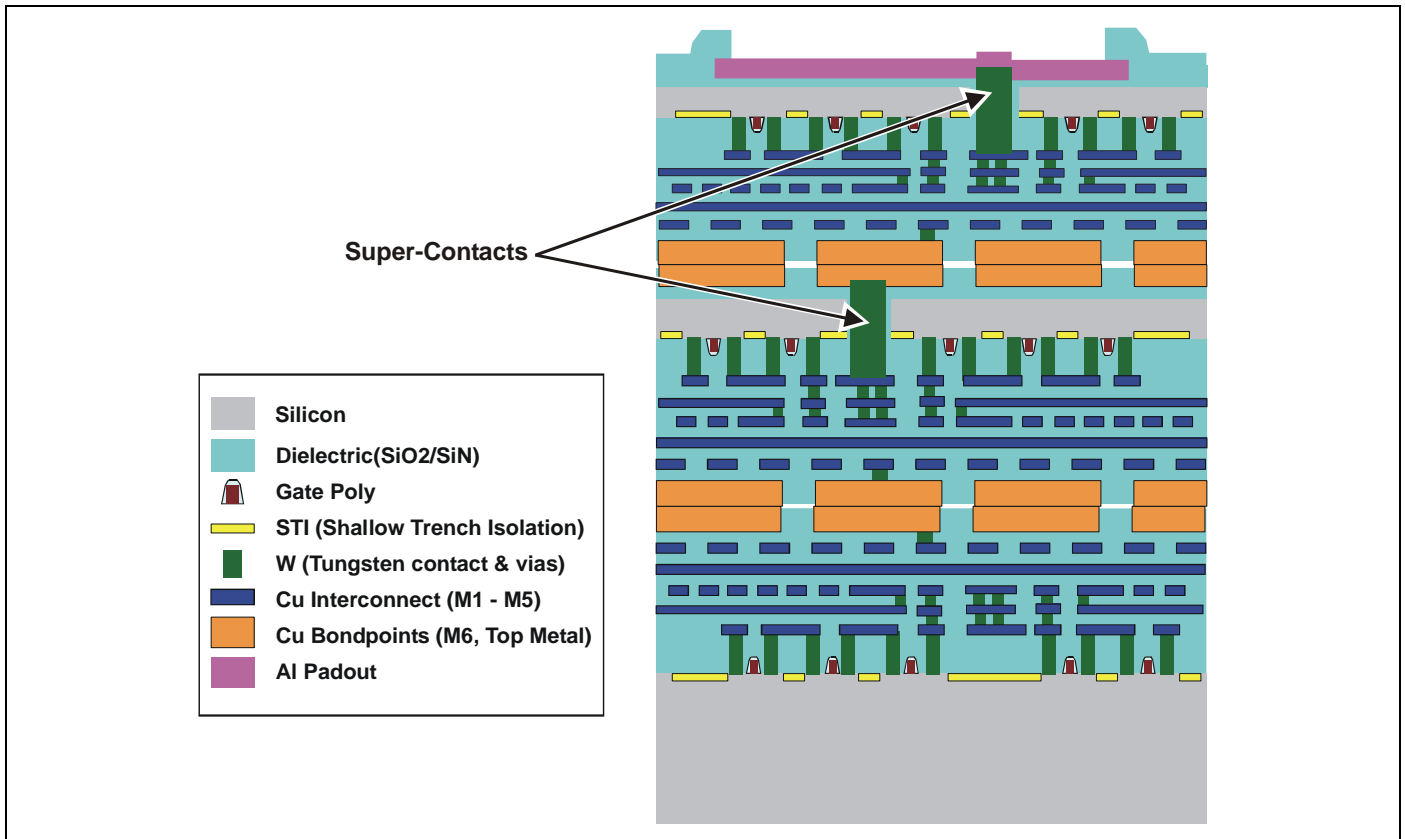
\* The bondpoint layer is formed by a copper single- or dual-damascene process.

# FASTACK® STACKING TECHNOLOGY



**Figure 1 – Cross-section diagram of two bonded wafers after thinning**

The back side of the thinned wafer, with its exposed Super-Contacts, can be metallized with bondpoints and bonded to the front side of a third metallized wafer. Thinning, metallizing, and bonding are repeated as desired. Once the wafer stacking process is completed, one side of the stack is thinned to the Super-Contacts and padded out for I/O; the other side is backlapped to remove excess silicon.



**Figure 2 – Cross-section diagram of a finished three-wafer stack**

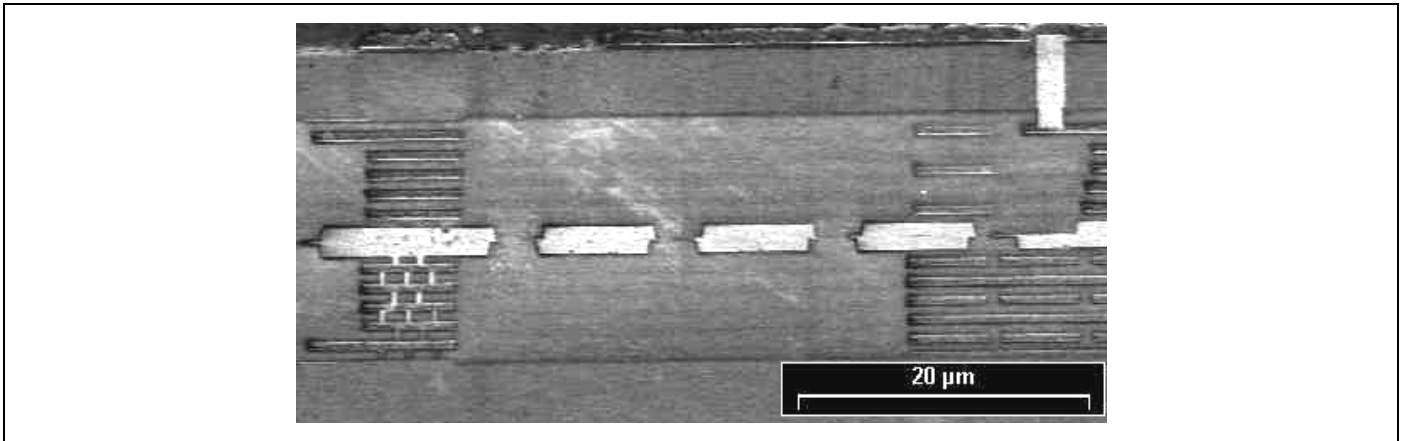


Figure 3 – SEM\* photo of a two-wafer stack.

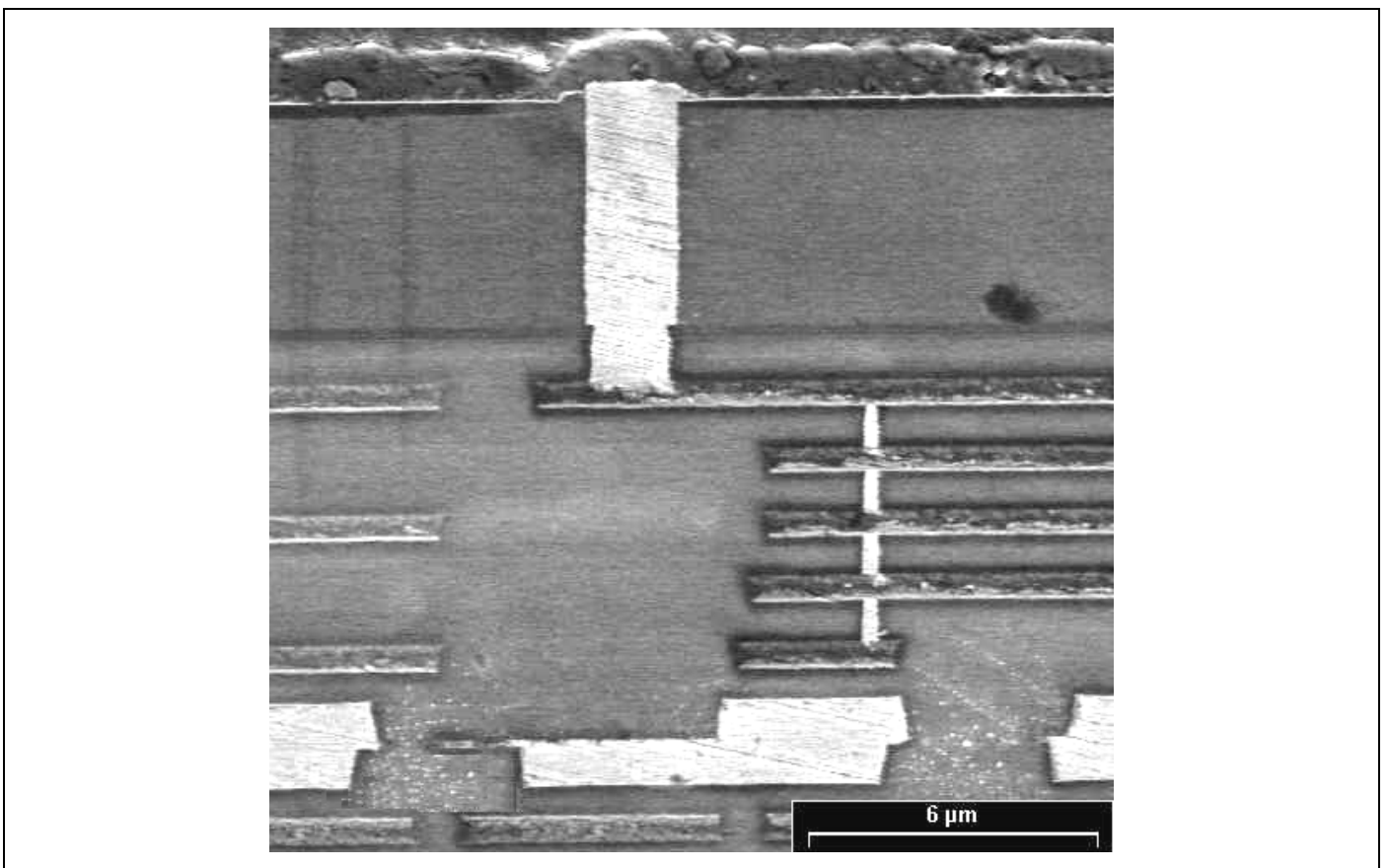


Figure 4 – SEM photo close-up of a Super-Contact.

\* SEM = scanning electron microscope

## Present Status of the Technology

Tezzaron built the first working 3D IC prototypes (six different devices) in 2004. In 2008 Tezzaron began producing custom stacked components under contract and now provides stacking services for a number of customers.

Tezzaron's process engineering group in Singapore continues to improve and refine the 3D stacking process. Some notable measurements:

- Super-Contact™ density can reach 160,000/mm<sup>2</sup> (typical designs use ~10,000/mm<sup>2</sup>)
- Alignment precision for 200mm wafers has a 3-sigma process tolerance of ±1 micron; precision of ±0.3 micron is typical
- Bond strength has been tested to a shear strength of more than 14 Kpsi (9.8 Kg/mm<sup>2</sup>)
- Ultra-thinning reduces wafer thickness to as little as 8 microns, uniform to within ±0.5 micron

## Summary

The FaStack process does not require exotic technology, yet it successfully addresses the three major stacking challenges:

- **Thermal buildup**  
FaStack's aggressive wafer thinning prevents excess thermal buildup and allows the stack to behave as one thermal unit; copper bonds facilitate heat dissipation.
- **Bonding**  
Tezzaron's wafer bonds have ample strength and uniformity.
- **Packaging**  
FaStack units are thin enough to mount in standard packages.

FaStack offers valuable benefits to the industry, producing 3D ICs that display measurable advantages:

- **Density**  
Each layer has the density of a conventional 2D chip, so total circuit density is multiplied.
- **Optimized Processing**  
Plentiful interconnects enable fine-grained circuit-level separation. For example, Tezzaron's FaStack DRAM cell wafers require 8 fewer mask steps than normal DRAM wafers.
- **Heterogeneous Integration**  
For example, DRAM process wafers are easily stacked with logic process wafers.
- **Speed/Power**  
High-density interconnects take full advantage of short vertical paths. The prototype FaStack 8051 processor runs at either 5x the speed of a normal 8051 or 10% of the power.

Tezzaron continually seeks new opportunities to apply this exciting technology and welcomes industrial and investment relationships.

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